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DESIGN OF A GE BASED FINFET FOR CPU SWITCH APPLICATIONS.

by

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"If you don't see the book you want on the shelf, write it."

Beverly Cleary

Abstract

The field of microelectronics experienced a huge shift from the traditional planar MOSFET to 3D multi-gated structures, most noticeable being the FinFET. FinFET is regarded the most favourable for progressing CMOS downscaling in the nanometer scale due to its ability to suppress short channel effects due to its better gate control, enabling it to achieve performance of high quality and low power. The fin dimensions play a huge role in the design of a FinFET. Looking at the gadget's Figure-of-merits, the geometries of the transistor are specifically delicate. In this work, a 30 nm Ge based FinFET is designed by parameter optimization which is achieved through parameter variation using Silvaco software. Literature where Poisson and Schrodinger equations were used to come up with a theoretical analytical quantum model, is used. The model is based on the quantum mechanical variational approach and accounts for the Ge channel thickness which depends on electric potential. Since the electrical characteristics are affected by design parameters such as doping concentrations, the most influential factors being on/off current ratio and threshold voltage, were determined through investigation of effects that arose due to variation of multiple design parameters. Systematical investigation is done with the help of graphical data such as current-voltage characteristics and mathematical models which include drain current model. Simulation results show that physical parameters in the form of fin dimensions also influence electrical characteristics of the device. It is also observed that $I_{ON/OFF} \approx 10^6 \text{ A}$ when the device operating in the range $0.05 \text{ V} \leq V_{GS} \leq 1 \text{ V}$. Properly scaling the drain and source depths and increasing the doping density for the oxide is mandatory in order to keep short channel effects in the form of DIBL minimal.

Acknowledgements

I would like to express my gratitude to my primary supervisor, Nonofu Ditshego, who guided me throughout this research. I would also like to thank my friends and family who supported me and offered deep insight into the study.

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List of Abbreviations

MOSFET	Metal- Oxide-Semiconductor Field-Effect Transistor
FinFET	Fin Field-Effect Transistor
CMOS	Complementary Metal- Oxide-Semiconductor
FET	Field-Effect Transistor
IT	Intergrated Circuit
VSLI	Very Large Scale Integration
SCE(s)	Short Channel Effect(s)
DIBL	Drain-Induced Barrier Lowering
HKMT	high-<i>k</i> Metal Gate
QME(s)	Quantum Mechanical Effect(s)
CAGR	Compound Annual Growth Rate
GAA	Gate All Around
BJT	Bipolar Junction Transistor
CFP(s)	Contention Free Period(s)
CMOS	Complementary Metal-Oxide-Semiconductor
DG	Double Gate
CPU	Central Processing Unit
SOI	Silicon-On-Insulator
MOS	Metal- Oxide-Semiconductor
TG	Tri Gate
ITRS	International Technology Roadmap for Semiconductors
DRAM	Dynamic Random Access Memory
QCSE	Quantum-Confined Stark Effect
HCI	Hot Carrier Injection
VDT	Voltage-Doping Transformation
2D	Two-Dimensional
3D	Three-Dimensional

Physical Constants

Speed of light	$c = 2.997\,924\,58 \times 10^8 \text{ m/s}$
Boltzmann constant	$k = 1.380\,648\,52 \times 10^{-23} \text{ J/K}$
Planck constant	$h = 6.626\,070\,15 \times 10^{-34} \text{ J}\cdot\text{s}$
Charge of an electron	$q_e = 1.602\,176\,62 \times 10^{-19} \text{ C}$

List of Symbols

L_G	fin/gate length	nm
H_{fin}	fin height	nm
t_{fin}	fin thickness	nm
L_D	diffusion length	nm
L_C	channel length	nm
q_f	fixed charge	C
n_i	intrinsic carrier concentration	cm^{-3}
m_x	effective mass of electron	kg
E_{ea}	affinity	J/mol
t_{OX}	gate oxide thickness	nm
q	charge	C
$n(x)$	electron density	$\text{e}/\text{\AA}^{-3}$
p_d or N_A	acceptor concentration	cm^{-3}
n_a	carrier concentration	cm^{-3}
Q_d	depletion charge density	C/cm^3
Q_{inv}	inversion charge density	C/cm^3
C_{OX}	oxide capacitance	F/cm^2
$I_{ON/OFF}$	current on/off ratio	-
V_{TH}	threshold voltage	V
G_O	yield conductance	S
Δf	frequency deviation	Hz
S	subthreshold swing	mV/dec
ε	permittivity	F/m
$\phi(x)$	surface/electric potential	V

*This work is dedicated to my friends and lovely brother,
Koorapetse John Mogosetso.*

Chapter 1

Introduction to Multi-Gated Field-Effect Transistors

The course of the human history has been changed by some great inventions like the discovery of fire and the invention of the wheel. One such invention is the introduction of semiconductors material which led to the great invention of transistors, and this had a huge impact on human civilization. This devices changed the way of life like no other technology. History is isolated dependent on the innovation utilized around then. Quite a long while from now, the discovery of semiconductors might be seen as one of the great demarcation lines of history. In correlation to some inventions that have been stated, the utilization of semiconductors is moderately new as the principal transistor made utilizing semiconductors was in 1947 [1]. There was a discovery by Moore several years after. About 70 years ago it took computers 70 hours to calculate the value of π up to over 2000 digits. Thanks to modern day computing power, with smartphones, the same task can be completed in blink of an eye, approximately 0.55 seconds. This incredible growth in speed was made possible by a turning device inside an electronic gadget called a transistor. The transistor used is the metal-oxide-semiconductor field-effect transistor (MOSFET). Smartphones have processors at the heart of their operation which have over a billion transistors [2–4].

The principal IC transistors were manufactured on "bulk" or mass silicon wafers until the start of the twentieth century when production changed to Silicon-on-Insulator (SOI) in order to address performance [2]. In these new sort of substrate, transistors are made in a slight silicon layer put over a silica layer. The selection of SOI substrates for assembling standard semiconductor items has given SOI research an extraordinary incentive. Previously, novel transistor structures proposed by SOI researchers were regularly viewed as odd and unreasonable, yet the ongoing achievement of SOI in the field of microchip assembling has at long last given this innovation it's believability and acknowledgment it merits. There are guarantees,

upgrades in both circuit speed and power utilization and on top of that, these gadgets offer the benefit of decreased parasitic capacitance and enhanced current drive [5–8].

MOSFET has been the driving force for the design of IC circuits since the inception of Moore's law in 1965 which anticipated that the number of transistors per chip would quadruple each 36 months [9]. This effective standard in microelectronics and semiconductor industry [10] led to the long history of the channel length of the MOSFET being scaled down to smaller dimensions which are now into the nanometre regime [11]. In the late 90s, scientists predicted that from 2010 manufactures will be able to create transistors with gate lengths equaling 20 nm regularly, which turned to be true [12]. This led to the evolution of silicon (Si) based MOSFET downscaling which has done really well regarding chip density and processing speed since the early sixties [13] [14]. To emulate the frantic pace forced by Moore's law, the microelectronics and semiconductor industry have been reducing the linear elements of the transistors to the point where we are now - nanometer regime. Under this dimensions, it is difficult to improve performance due to severe short channel effects (SCEs) [15].

A large number of solutions have been tried over the years, most common being a fabrication of multi-gate MOSFET structures [16] and application of high dielectric metal gate (HKMG) [17–19]. In order to meet the ever increasing demand for higher operating speed the industry has to come up with ways to overcome SCEs while on the hand increasing drive current. This has led to the shift of focus from classical single-gate transistor structures to multiple-gate MOSFET architectures [20]. Multi-gated MOSFET devices include double gate (DG), tri-gate (TG) and gate all around (GAA). Although almost all multi-gated MOSFET structures have better gate control when compared to their planar counterparts, the tri gate MOSFET is the most reassuring structure for CMOS scaling to nanometer magnitude due to its capability to hold back SCEs [21]. Fin field-effect transistor (FinFET) is a summed up term used for any field-effect transistor (FET) utilizing a semiconductor, popularly silicon, fin as body built over an oxide substrate. Fundamentally GAA cannot be categorized as a FinFET while tri-gate MOSFET is one of the FinFET implementations. GAA is a major revamp of the conventional MOSFET design in which gate electrode surrounds the silicon-based channel on four sides rather than three, as utilized in contemporary FinFET gadgets. A progressively proper term would be tri-gate FinFET since lately MOSFET is popularly associated with non SOI structures like bulk MOSFET. Just like other multi-gated devices, FinFET technology is highly recommended as an alternative for CMOS to suppress limitations brought

forth by the vigorous downscaling [22–24].

Another scaling limitation on top of SCEs is tunneling which is a standout quantum mechanical effect. As the feature dimensions of the complimentary metal-oxide semiconductor (CMOS) technology are scaled down to smaller lengths on the sub 10 nm scale, quantum mechanical effects (QMEs) become prominent [25]. Because of essential material and process innovation limits, challenges such as reducing the SCEs and QMEs, limiting the leakage current, and lessening the gadget-to-gadget variability have been presently ruining the regular improvement in the circuit speed and the expense per functionality brought fourth by the traditional scaling down of the dimensions of transistors underneath 22 nm over the recent years [26] [27]. As it was stated earlier, FinFET, one of the sub nano multi-gated gadgets [28], is deemed the best technology to extend CMOS downscaling to the sub-10 nm regime [29]. Predominant scalability, minimal gate leakage current, magnificent control of SCEs to guarantee higher short channel accomplishments, relative immunisation to the gate line-edge roughness, being compatible with the current technologies and most importantly better gate control are the key properties of this device [30–35]. It was show in the earlier studies that the fin dimensions are very critical when generating the enhanced drive current along with threshold voltage (V_{TH}) [36] [37] hence performance can be improved by varying the geometries of the fin while cautiously paying attention to any trade-offs in current and threshold voltage [38].

Germanium (Ge) is regularly utilized for high performing devices as an alternative to silicon (Si) due to its high carrier mobility on top of a hole mobility which is double of silicon [39–41]. Literature says [42] the main setback for a Ge based FinFET is a very low threshold when compared to Si, which in time leads to SCEs due to the fact that devices turn on too fast resulting in high delay time. The main aim of the research is to design a Ge FinFET so that it operates with high performance and efficiency. In this work, a 30 nm Ge FinFET is designed by parameter optimization which is achieved through investigation of multiple design parameters and assessing their effects in order to determine a parameter which has the most influence on the device.

The rest of this research is organised as follows. Chapter 2 gives a background on multi-gated MOSFET structures. Chapter 3 presents the theory of field-effect transistors (FET). Chapter 4 presents the design specifications for Ge based FinFET (tri-gate FinFET) together with the models used and simulation details. A double gate (DG) MOSFET quantum analytical model is used to study the behaviour of the

device alongside the drain current model. Chapter 5 is presentation of results and discussions while conclusions are drawn in Chapter 6.

1.1 Motivation

Since their discovery at Bell Laboratories many years ago, transistors have driven the semiconductor industry as the primary component of electronic circuits. It is not an overstatement to say that the transistor's emergence into electronic circuits enabled modern microelectronics structures, computerization, wireless communications, space travel, and modern science and research in general. About ten years after the transistor's creation, the advancement of ICs ushered in a new era for transistor electronic applications circuits. Since the introduction of the first integrated circuits, the market has demanded ever-increasing functionality per package component. To meet this demand, the manufacturing sector is expanding the amount of transistors per chip. Naturally, manufacturing sector, on the other hand, continues to keep production costs as low as possible. Downscaling transistors is considered to be the best case to meet the increasing demand for a large number of transistors placed in a single chip. The concept of scaling traditional transistors, and that is the general concept of this research, then gathered momentum, threatening to transform the development of the microelectronics industry.

1.2 Problem statement

FinFET structure was brought forth to improve the planar Si-MOSFET scaling issues which hindered gadget scalability. The technology also suppresses off-state leakage current. However Si based FinFET just like the planar Si MOSFET has reached its critical scaling and performance limitations. The main ultimate limitation to the scaling of transistors is the atomic structure [43] of matter. A MOSFET cannot be smaller than an atom. With vigorous downscaling in the nanometer regime, quantum mechanical effects become prominent [44]. Standout quantum mechanical effect is tunnelling [45], where the electrons tend to travel through a hindrance or a barrier that they classically shouldn't almost certainly travel through. This effect fully show that the depletion layer widths should indeed always be greater than the transistor channel width otherwise there will be a negative depletion layer leading to the flow of tunnelling current. Ge is regularly utilised for high performing devices as an alternative to Si. Very low threshold potential which is the source for fast turning-on of devices is a standout setback for this device [42]. This major setback

eventually also leads to high SCEs which result in high delay time, thus diminishing the switching speed. Also for Ge based devices, quantum confinement effects such as quantum-confined stark effect (QCSE) always arise [46]. Quantum confinement arise due to the confinement of moving electrons in the Ge film. Study of the movement of electrons in the Ge-film has shown that electrons move randomly but restricted in specified energy levels in quantum wells [47]. In this way an analytical model is required to plan future integrated circuits (IC).

1.3 Aim

The main aim of the project is to design a germanium based FinFET by parameter optimization so as it operates with high performance and efficiency.

1.3.1 Specific objectives

In order to achieve the main aim of the project, the following objectives have to be followed:

- To design sub-0.1 μm germanium based TG MOSFET.
- To vary multiple design parameters guided by theoretical equations.
- To investigate how each design parameter influence device behaviour.
- To optimize each parameter value by comparing how its variations affect the design and then comparing the optimized parameters with the state-of-the-art Si-FinFET device.

1.4 Justification of study

Because of the widespread need for electricity in our today's life, transistors can now be found in virtually every electronic circuit. Transistors are needed in our daily lives in a variety of ways, including amplifiers and switching apparatus. They are being used as amps in various oscillators, modulators, detectors, and almost any circuit to execute a role. The MOSFET is the fundamental component of too many modern electronic devices and serves as the foundation of modern electronics. It's also the most common popular transistor in electronics and the most commonly used semiconductor device throughout the global economy. It has been referred to

as the "workhorse of the technology sector" and "core innovation" of the late twentieth to early twenty-first centuries. Since the sixties, CMOS scaling and miniaturization were always the key drivers driving the accelerated massive growth of electronic semiconductor devices, with fast miniaturization of MOSFET being majorly crucial for stimulating transistor density, improving performance, and reducing energy usage of semiconductor chips and electronic equipment. Since the goal is to keep transistors as small as possible, the question is how small they can get and when they can no longer be reduced in size. Another intriguing aspect is whether changing the material used in MOSFETs can help reduce energy consumption and improve performance.

1.5 Publications

To date, there are two publications related to this research project (conference and journal). The first one has been published in BIUST Research & Innovation Symposium And Stem Festival 2019 while the latter is under review at JES1 (Journal of electrical systems).

1. Gofaone Mogosetso, Caspar K. Lebekwe and Nonofu M. J. Ditshego, "Design of a 30 nm Germanium FinFET by Parameter Optimization," *Advanced Engineering Forum*, vol. 44, 2021.
2. Unopa Matebesi, Gofaone Mogosetso, Caspar K. Lebekwe, W. H. Khoo, S. M. Sultan, N. M. J. Ditshego, "IGZO TFT versus the MOSFET," in *BIUST Research & Innovation Symposium And Stem Festival 2019 (RDAIS 2019)*, ISSN: 2521-2292, page 54 – 58, June 2019.
3. Attended a Research & Innovation Symposium And Stem Festival 2019 held June 3rd to 7th, 2019.

Chapter 2

Background

MOSFET falls under the field-effect transistor (FET) category, the other being bipolar junction transistor (BJT) [48], the former being the most commonly used transistor in the world. Unlike BJTs, MOSFET have a scalable nature which means a lot of them (millions) can be fabricated in a single wafer [2]. Other formidable differences include the fact that MOSFET operates with one type of charge carrier, either hole or electron, which makes them less noisy [8]. A transistor can either be used as a switch or an amplifier. The former being the main property exploited in the micro-electronics and semiconductor industry. This property of the transistor opens the doors to the world of digital memory.

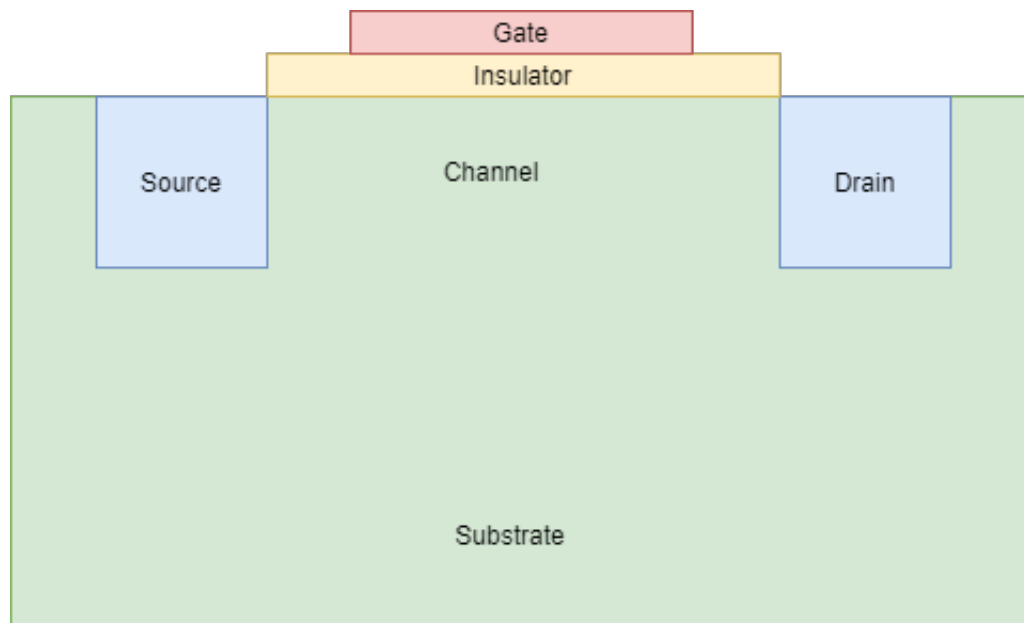


FIGURE 2.1: A MOSFET structure

Each silicon wafer is made up of dozens and dozens of chips, each chip is made up of millions of transistors, and each transistor is combination of two regions known as the "source" and "drain". Figure 2.1 shows the simple and general structure of a MOSFET. A four terminal (drain, source, gate and the body) 2D device.

Figure 2.2 displays a more detailed structure, the popular n-channel (NMOS) silicon (Si) MOSFET. The two n-type areas in NMOS are separated by a p-type region known as the substrate. PMOS devices are built differently, with the two regions being p-type and the substrate being n-type. A thin sheet of insulator material encompasses the region between the source and the drain, and above it is a metal electrode, which gives rise to the term "metal" in the name metal-oxide semiconductor field-effect transistor, and it is referred to as the gate. The insulating barrier is an oxide, normally silica/silicon dioxide (SiO_2), even though other materials can be used such as high- k dielectrics based on applications. V_G is voltage applied to the gate while voltage applied at the source and the drain contacts is denoted V_S and V_D respectively.

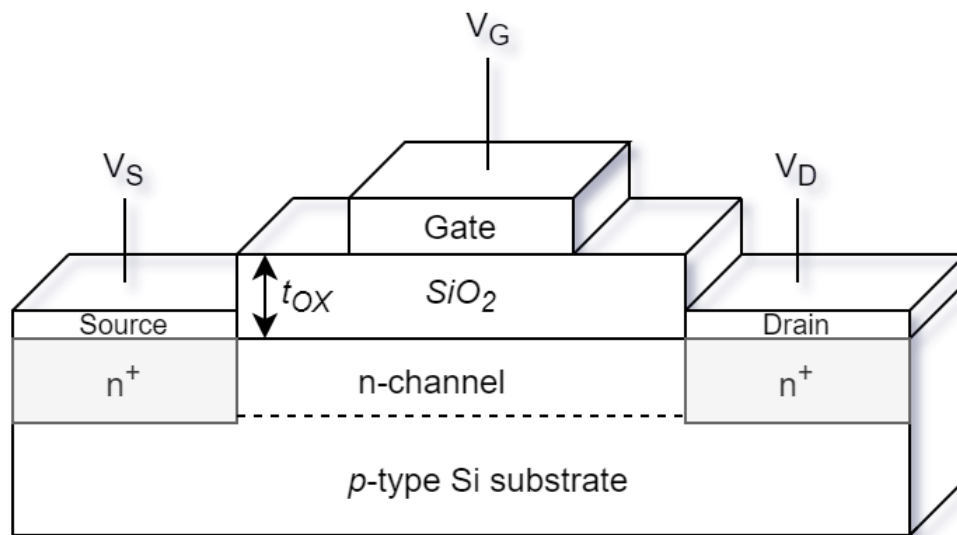


FIGURE 2.2: Detailed diagram of the MOSFET

Whenever a certain voltage is applied to the gate, an electron stream forms between the source and the drain, allowing the whole device to function as a current source governed by voltage (voltage controlled source) [49] [50].

2.1 Semiconductor Basics

Semiconductors are materials which can act either as an electrical encasing or conductor dependent on the conditions in which they work. This conduct is because of two electrical properties being the bonding properties of the individual atoms which structure a bulk material and the interactions between their external electrons. Similarly like all other atoms, the individual atoms of semiconductors materials have a set structure that decides their way of bonding with different atoms.

2.1.1 Atomic Structure and Quantum Theory

An individual atom comprises of protons, neutrons and electrons. Protons and electrons are positively and negatively charged respectfully, while neutrons have no charge. The structure is held compact by the alluring forces of the oppositely charged protons and electrons. The central nucleus of an atom comprises of protons and neutrons and it is circled by a cloud of electrons. This electron cloud is comprised of quantized shells that have a certain energy level. Each electron in this circling cloud should stay at a quantized energy level. An electron can move to a higher energy shell by engrossing energy or drop to a lower shell by exuding energy. The alignment of quantized shells is the most significant deciding factor in relation to how the atom will interact with other atoms making this an electrical property [51–53].

In each atom, every electron has a distinctive combination of quantum numbers which portray its energy state in the atom. The quadruple quantum numbers are denoted by the letters n , l , m , and s . n which is the first number, denotes the shell that the electron holds. For a higher energy state, a higher shell level is required and the same applies to lower energy state which means lower shell levels have electrons in lower energy states. The l and m numbers indicate sub-shells that show up inside each shell and each can carry two electrons of opposite spin. The s number which can either be negative or vice versa denotes the spin of the electron [52–56]. Table 2.1 derived using [57] and [58], is the summary of the potential values of each quantum number.

TABLE 2.1: Potential outcomes of all the quantum numbers

Quantum Number	Possible Quantum Number Values
n	$n = 1, 2, 3, 4, \dots, n$ where n correlate to the energy level of the outward shell
l	$l = 0, 1, 2, 3, \dots, n - 1$
m	$m = l, l + 1, \dots, l - 1, l$
s	$s = -\frac{1}{2}, +\frac{1}{2}$

2.1.2 The Crystal Lattice

Each rigid material is comprised of individual atoms coordinated in a specific way and can be categorized amorphous, crystalline, or poly-crystalline dependent on

the arrangement (see Figure 2.3) [59]. The most plentiful solids discovered naturally on the earth are typically amorphous, which means their individual atoms are not set orderly. For a crystalline material, the arrangement of atoms is periodic and it is termed a crystal lattice, which is sustained all over the solid. Consequently, the solid seems the same when analyzed at the atomic level anytime. Materials that don't fall into either the amorphous or crystalline classification are named poly-crystalline. Poly-crystalline materials are made out of various regions which each have a cyclic ordering of atoms, yet the entire material isn't uniform in its arrangement [59] [60].

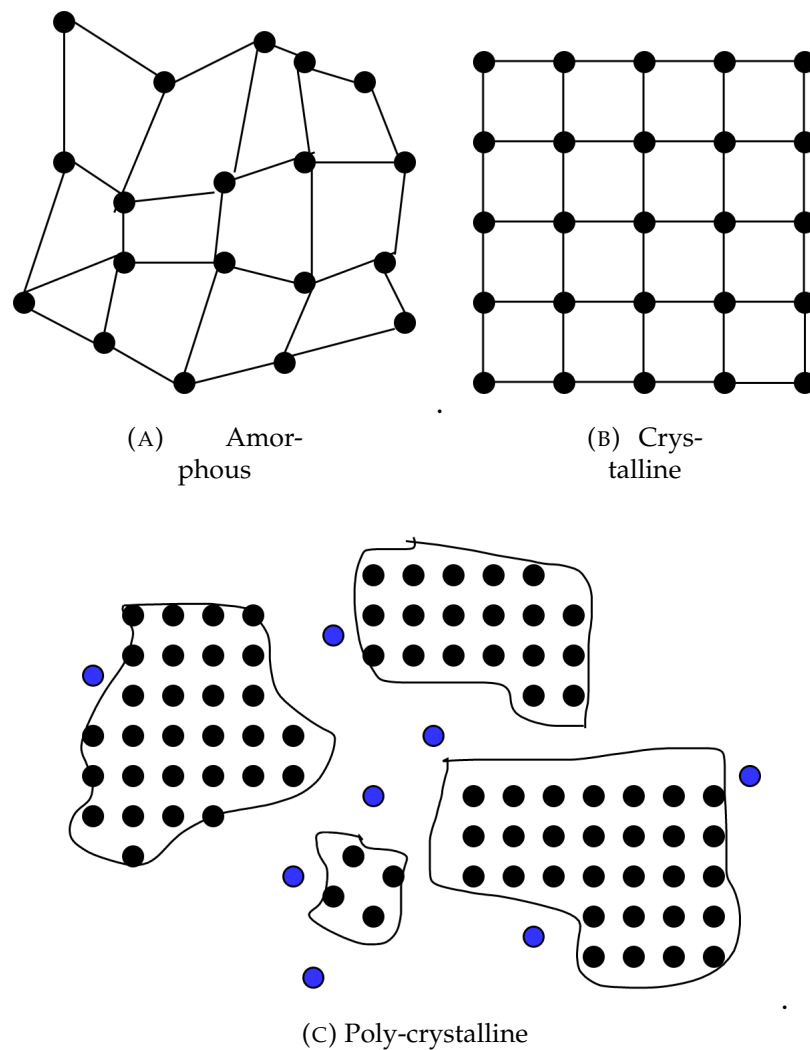


FIGURE 2.3: Basic lattice structure of amorphous, crystalline and poly-crystalline

Crystalline solids, which are the most regularly utilized materials in solar cell applications, can be additionally characterized dependent on the sort of layout of their crystal lattice [60]. Each lattice can be decreased to a unit cell, a little volume that is illustrative of the entire cell. This unit cell shapes a geometry which can take numerous forms. The most regular structures are the differentials of the cubic and

diamond lattices. An illustration of a diamond crystal lattice is given in Figure 2.4. The diamond lattice is displayed with each dark spot standing in for each separate atom and every solid line showing a bond between atoms [60–62]. A material can be considered as an enormous item made out of huge amounts of these unit cells set up as building blocks.

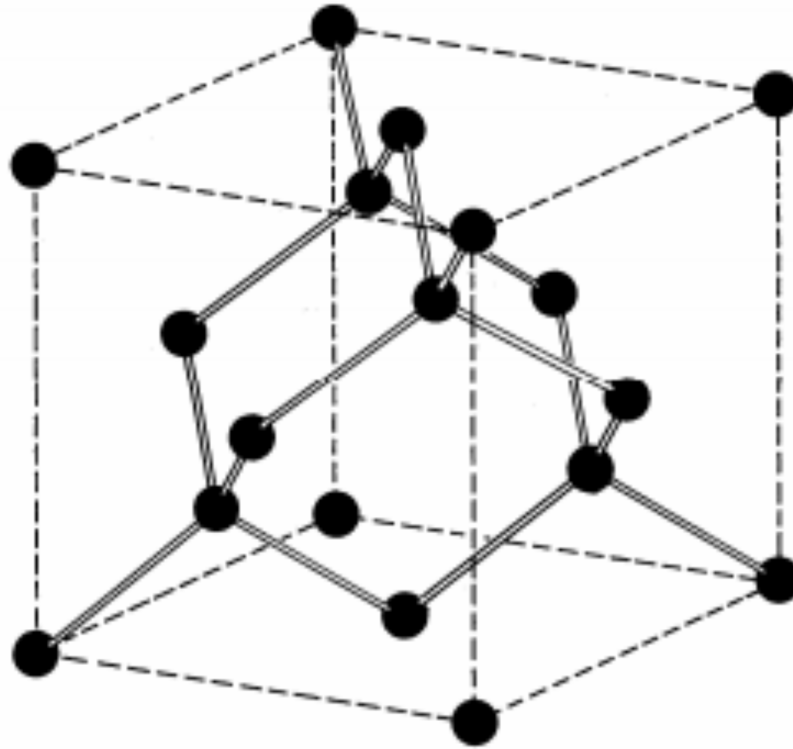


FIGURE 2.4: Diamond lattice

In regard to solar and electrical applications, the unit cell structure of a semiconductor material decides large numbers of its significant properties [63]. The numbers and kinds of bonds between atoms of the material decide the attributes and features of the progression of charge carriers in the material, characterizing variables like resistivity and conductance [52]. The order and structuring of the atoms likewise decides if particular materials can be developed in layers adjacent to one another to fabricate a specific. There is a situation where the lattices of two adjacent materials can't form a suitable electrical interface because of clashing lattice structures. This condition is called lattice mismatch, where two material lattice structures don't coordinate in a certain way [60–63]. These properties controlled by the crystal lattice join with the properties and structure of the individual atoms to give each material distinctive properties.

2.1.3 Energy Bands

Similarly that electrons can just dwell at particular quantized energy levels in an individual atom, they are limited to occupying energy bands in a solid [52]. Be that as it may, each of these energy bands is comprised of a scope of energy levels which each electron can inhabit. This distinction emerges from the impact of all adjacent atoms on an electron. On account of an individual atom, an electron dwells in a quantized shell with a related energy level [64]. If two atoms are sufficiently close to one another, their electrons and other alluring forces will impact one another, making distinctive energy states in particular bands of energy [64]. In the band outline in Figure 2.5, inter-atomic distance is plotted against electron energy. The band outline indicate that when atoms of a similar component are endlessly far away from one another, they have a similar quantized energy levels [65]. Nonetheless, when the atoms are nearer together, the electrons of each atom interrelate, and the discrete energy levels separate into a band of permitted energies displayed by the shaded part of the graph in Figure 2.5 [65] [64].

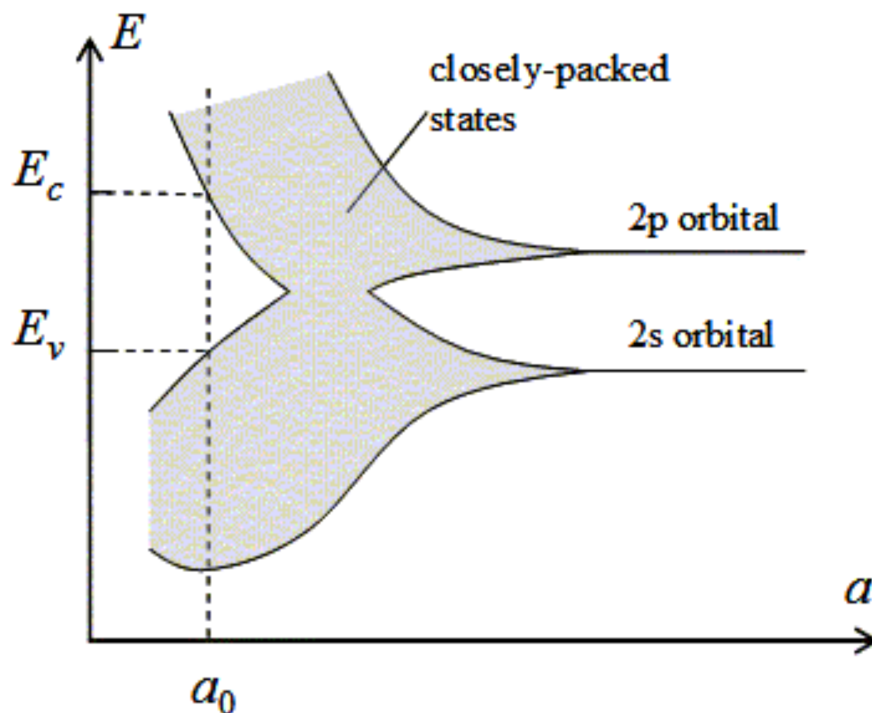


FIGURE 2.5: Inter-atomic separation vs energy to display the information of energy bands in a material

The solitary energy bands of significant worry in MOS applications are the valence band and the conduction band [66]. The valence band is the furthest energy shell of every atom. The electrons in this band are normally detained in place by

bonds between atoms. In the event that an electron in the valence band gets energy bigger than or equivalent to the distinction in energy in the conduction and valence band, regarded as the band-gap, at that point it will move into the conduction band. At the point when it moves into the conduction band, the electron splits from its bond and turns into a free electron in the material. An electron can possibly climb to the conduction while acquiring energy in the valence band in light of the fact that there are no permissible energy states for an electron to involve inside the band-gap [64] [65].

The capability of the material to conduct electricity is determined and influenced by its band-gap [64] [65]. For insulators, the band-gap is comparatively big and it needs a huge amount of energy to excite free electrons. On the other hand, semiconductors have relatively little band-gap and this allows them perform as insulators or conductors subject to the energy level of that material. Conductors have free charge carriers in absence of inclusion of outside energy due to overlapping valence and conduction bands [64] [65]. Figure 2.6 shows that the band-gap is inversely proportional to conduction capability.

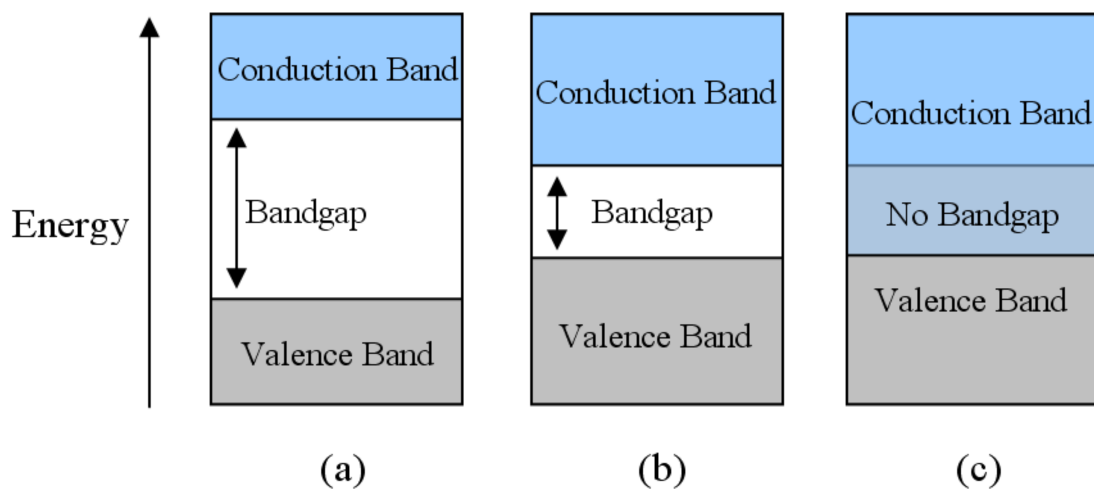


FIGURE 2.6: The relative band-gaps of insulators (a), semiconductors (b) and conductors (c).

Semiconductors exist with a tolerable band-gap as a result of the distinctive state in their valence bands [66]. Each and every elemental or single element semiconductor consist of four electrons in its valence band. These elements are termed group IV components. The atoms of these materials bond with one another to fill the external shell of each one of the encompassing atoms by the utilization of four covalent bonds with atoms in close proximity [52]. These covalent bonds can be separated by bringing in energy, which in turn, loosens charge carriers. Further semiconductors

are comprised of compounds in which the two element's valence electrons add up to eight. This can be accomplished in various basic elemental combinations to make powerful and effectual semiconductor materials [59] [51].

2.1.4 Charge Carriers

At the point when bonds are broken in a material because of the assimilation of energy, two various sorts of charge carriers are made up called electrons and holes. Electrons are essentially the negatively charged elements of atoms and are viewed as free electrons when they split away from a bond. Holes are contrarily the positive charge gave up by the split bond of the free electron. In contrast to free electrons, holes exist in the valence band. Holes are not actual particles but rather are just positive charges made by the absence of vital electrons for charge balance. In spite of the fact that holes are not actual particles with a mass, their flow is related with a value of current that is greater than zero while electron stream is related with negative current [54] [56].

Charge carriers (electrons and holes) each have a related mobility in every material dependent on how effectively the free charge carriers can travel through the material [52]. In spite of the fact that electrons and holes are of equivalent charge, electrons have a bigger mobility. Electron and hole mobility of a certain material is reliant on numerous material qualities, for example, the lattice structure, atomic size and the channel orientation of the material in which an electron or hole is moving [60] [55]. The charge carrier mobility decide parameters like the conductance and resistivity of a material, which are significant variables in CMOS VLSI [12] [67].

2.1.5 Doping

Doping is the cycle of deliberately bringing impurities into a semiconductor material to control its electrical attributes. An one hundred percent, undoped semiconductor is termed intrinsic, while a doped semiconductor is termed extrinsic. A semiconductor can be doped with either p-type or n-type material. The p-type dopants, termed acceptors, have the number of valence electrons less or equal to three. This kind of dopant bonds with all the neighboring atoms but needs sufficient electrons to completely fill its external shell. Accordingly, it draws in electrons, instigating the generation of holes in the material. A n-type dopant, called a donor, has at least five valence electrons, permitting it to completely bond with the entirety of the surrounding atoms while leaving off an extra, unbonded electron. This electron can simply be excited into the conduction band since it isn't limited by the energy of

a covalent bond. The additional charge carriers made by doping can considerably expand hole or electron concentrations, permitting the creation of materials more fit to most applications than intrinsic semiconductors [22,27,45,68,69] .

2.1.6 The P-N Junction

The majority of the uses of semiconductors, including FET, are conceivable due to the properties made by the intersection between a p-type region and a n-type region. The region where these two materials meet is known as a p-n junction and works as a diode. In this region, surplus electrons in the n-region and surplus holes in the p-region diffuse across the boundary of the two regions to create a depletion region in which oppositely charged particles make a hindrance that obstruct charge flow. The development of the depletion region from the junction of p-type and n-type materials is made possible by the behaviour of the electric field which opposes and blocks the electric flow in the depletion region [2,6–8,69].

The moment the materials meet, the surplus carriers on each material's boundary transfers to the next material, pulled in by the holes or electrons on the opposite side of the junction. These charges leave behind ions that at that point have a negative charge on account of the p-side and a positive charge on account of the n side. This hindrance at that point restricts charge flow in light of the fact that the electrons on the n side are repelled by the negative region on the edge of the n-side and the inverse is valid for the holes on the p side. In the event that the junction is forward biased with a voltage higher than the potential of the depletion region potential, at that point the diode conducts current. In the event that the diode is reversed biased, it goes about as an insulator and the depletion region grows [53] [55].

2.2 Scaling Issues

Performance enhancement has been troublesome on account of the limits of traditional planar MOSFET scaling which led to the gradual development of the SOI MOSFET from partially depleted, single-gate devices to multi-gate, fully depleted structures. FinFET structure was brought forth to improve the planar Si MOSFET SCEs which hindered gadget scalability and the technology also suppresses off-state leakage current. However Si based FinFET just like the planner Si MOSFET is beginning to experience critical scaling difficulties. The main ultimate limitation to the scaling of transistors is the atomic structure of matter. A MOSFET cannot be smaller

than an atom [43, 44, 70, 71]. With vigorous downscaling, quantum mechanical effects become more prominent, particularly in the nanometer regime. Multi-gated FET structures are taken as a way around these limitations. As more Moore's law predicted, as time elapses so are the linear dimensions of the transistor. The question is why should transistor's dimensions be reduced at this frantic pace. Several answers to this questions include:

- Larger chips have a larger surface area. With the speeds that people require nowadays, it is concerning how long it will take an electrical signal to travel from one side of a chip to the other. The clock cycles must be less than a nanosecond. In [72], QPI in Intel microprocessor delivered up to 25.6GB/s BW per port at 6.4GT/s.
- Smaller transistors allow for more of them to be packed onto the same die. More transistors mean more processing power. Intel nor longer state the number of transistors per chip but an estimation can be made using the popular "transistor density metric" which uses mega-transistors per millimeter square (MTr/mm^2). IBM declared its Research Alliance accomplices, including Samsung and GlobalFoundries in June 2017, had made a procedure to make 5nm chips utilizing Si nanosheet transistors and that new innovation, reported 2 years after their 7nm leap forward, would help to rise density from 20 million to 30 million transistors on a fingernail-sized gadget. According to WikiChip, Intel dual Core (i3/i5/i7) has over 1.75 billion transistors per $101.3mm^2$.
- Small transistors mean less power will be consumed. Small transistor means a small gate, which means less capacitance (C_{OX}).
- If transistors are small, many of them can be made on a single wafer. In this manner production will be cost effective

Intel has been bossing micro-chip industry with their 3D TG-MOSFET which replaced the planar MOSFET in 2011. The device was manufactured at 22nm and this shows there is gap in the industry as today researchers are looking below 10nm for both L_G and t_{fin} . In short transistor size and structure are a key innovation mainstay of conveying the advantages of Moore's Law to the end client [12]. The littler and more power effective the transistor, normally the better. Intel which right now for the most part of this paper will be used as a case study because of its prosperity and merits in the microchip business proceeds to typically shrink its assembling innovation. Table 2.2 shows a scaling migration of Intel over the years.

TABLE 2.2: Scaling migration of Intel

Dimension	Year	Key attributes
45 nm	2007	The transistor included high- k /metal gate.
32 nm	2009	The last 2D transistor presented to the international market by Intel.
22 nm	2011	The world's first 3D transistor for high volume logic process.
14 nm	2014	second Generation 3D tri-gate transistors.

Consistent transistor innovation advancements, empower Intel to make significantly powerful processors with unbelievable power effectiveness.

2.2.1 Moore's Law

In 1965 Gordon Moore issued his well known paper which illustrate the advancement of the transistor density in the integrated circuits. He anticipated that the quantity of transistors per chip would quadruple each 36 months [9]. This forecast ended up known as Moore's law and has been amazingly pursued by the semiconductor business since the 1960s.

After 1990, companies involved in the semiconductor business together with the scholarly community have collaborated to foresee more precisely the fate of the semiconductor industry. This activity brought forth the International Technology Roadmap for Semiconductors (ITRS) organization. The ITRS gives out a report yearly [12], which acts as a benchmark for the semiconductor industry. These reports depict the sort of technology, equipment, instruments and metrology devices that must be created so as to keep pace with the exponential advancement of semiconductor gadgets anticipated by Moore's law. Figure 2.7 demonstrates the development of the quantity of transistors per chip anticipated by the ITRS 2005 for highly performing processors and dynamic random access memory (DRAM) in the micro-electronics industry.

Si complementary metal-oxide-semiconductor (Si-CMOS) has been the pillar of the semiconductor industry since the early sixties [13] [14] due to its building block,

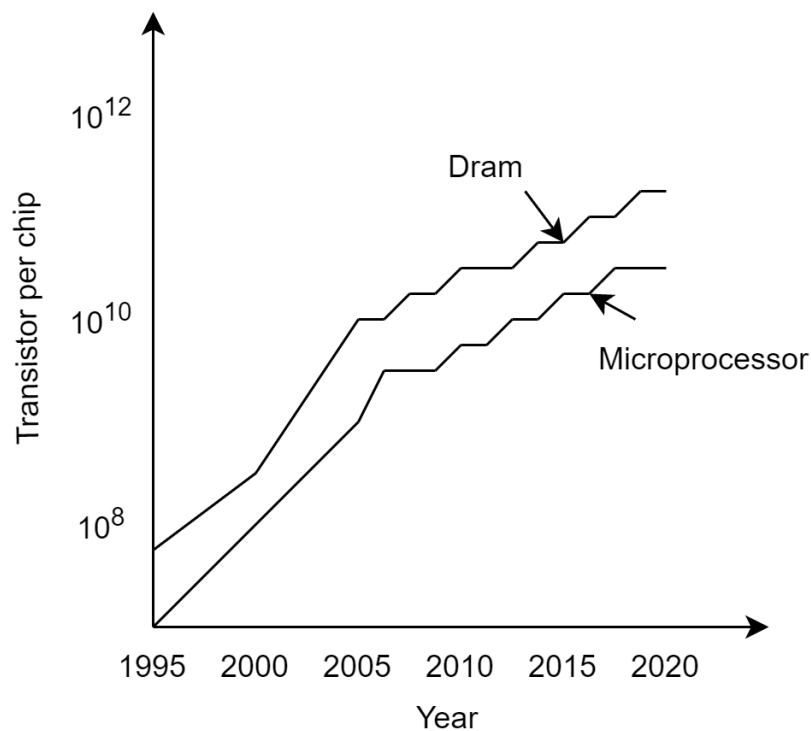


FIGURE 2.7: Moore's law: A prediction by the ITRS 2005 for DRAMs and high-performance microprocessors

MOSFET. So as to emulate the frantic pace forced by Moore's law, the linear elements of transistors have diminished significantly at regular intervals, to be precise, nerly 50% every 3 years [12]. In the late 90s, scientists predicted that in 2010 manufactures will be able to create transistors with gate lengths equalling 20nm regularly [12]. The principal integrated circuit (IC) transistors were manufactured on "bulk" or mass silicon wafers until the start of the twentieth century when production changed to Silicon-On-Insulator (SOI) in order to address performance. The new sort of manufacturing guarantees upgrades in both circuit speed and power utilization and on top of that, these gadgets offer the benefit of diminished parasitic capacitance and enhanced current drive.

2.2.2 Short Channel Effects

As the elements of transistors are contracted, the gate electrode is unable to control the potential dissemination and current flow in the channel area due to the fact that the nearness between the source and the drain lessens. As a result unwanted effects known as short channel effects (SCEs) start tormenting MOSFET [69]. It is difficult to shrunk the dimensions of traditional "bulk" MOSFET to very small lengths, more especially beneath 20nm. This implies the achievement that was picked up

by downscaling the Si-MOSFET has ended [68]. This impediment likewise implies the finish of Moore's law and the industry needs to figure out how to overcome it. Extreme SCEs which include drain-induced barrier lowering (DIBL), velocity saturation and hot carrier injection (HCI) in transistors lead to terrible performance prompting unreliability and making it difficult to improve execution in devices [15] [73] [74].

To overcome SCEs, many design aspects were changed. A typical example would be increment of the doping concentration in order to decrease the depth of the channel region, thus automatically reducing the depletion depth. For a long time, designers and researchers have been working tirelessly to come up with fabrication processes that would ensure minimal or no SCEs. Several solutions that relates well with the propelling fabrication techniques have been brought fourth, for example, high-k metal gate [17] [18] and multi-gated devices such as FinFETs. The idea is that these techniques ensure continuation of Moore's Law.

Voltage-Doping Transformation (VDT) model [75] is a tool that can be utilized to convert the effects of contracting gadget parameters, for example, gate length or drain voltage into electrical parameters. In a specific case the VDT model can be used to derive the following relation [76]:

$$SCE = 0.64 \frac{\epsilon_{Ge}}{\epsilon_{OX}} \left[1 + \frac{x_j^2}{L_{C_{eff}}^2} \right] \frac{t_{ox}}{L_{C_{eff}}} \frac{t_{dep}}{L_{C_{eff}}} V_{bi} \equiv 0.64 \frac{\epsilon_{Si}}{\epsilon_{ox}} EIV_{bi} \quad (2.1)$$

To be more specific, Equation 2.1 can be used to derive another expression for DIBL where

- $L_{C_{eff}}$ is the effective channel length
- V_{bi} is the source/drain built in potential
- t_{ox} is the gate oxide thickness
- x_j is the source and drain junction depth
- t_{dep} is the depth of the depletion region
- EI Electrostatic Integrity factor

$$DIBL = 0.8 \frac{\epsilon_{Si}}{\epsilon_{ox}} \left[1 + \frac{x_j^2}{L_{C_{eff}}^2} \right] \frac{t_{ox}}{L_{C_{eff}}} \frac{t_{dep}}{L_{C_{eff}}} V_{DS} \equiv 0.8 \frac{\epsilon_{Si}}{\epsilon_{ox}} EIV_{DS} \quad (2.2)$$

The value of EI rely on the geometry of the device and it can be used to determine the effect of electric field padded from the drain on the depletion region. This is one of the major causes of the SCEs, specifically the DIBL effects. Provided the $L_{C_{eff}}$ is known, equation 2.1 and equation 2.2 can be used to draw up the relationship between threshold voltage and the SCEs.

$$V_{TH} = V_{TH\infty} - SCE - DIBL \quad (2.3)$$

If the gate length is shrunk at the same time with the threshold voltage, the resulting SCE is called the threshold voltage roll-off. The mathematical expressions show that SCEs can be limited by lessening the:

- junction depth.
- gate oxide thickness.
- depletion depth.

2.2.3 Quantum Mechanical Effects

Quantum effects are getting progressively articulated at the most advanced nodes, causing strange and once in a while startling changes in how electronic gadgets and signals act. More often than not quantum effects regularly happen unnoticed for a large portion of the chip business. As structures are scaled further down to smaller lengths on the sub-nano-meter scale, let say 5 nm or less, quantum effects are rising as an increasingly broad and critical issue [45]. Quantum effects have been researched for quite a long time and not simply in the semiconductor business. Quantum tunneling, for instance, has been recorded for almost a century in alpha particle decay study. Yet, in the chip world, these quantum effects appear in an assortment of bizarre practices that are getting progressively problematic.

Flash memory was one of the primary places that chip producers started encountering quantum effects firsthand. Starting quite a long while back, NAND memory organizations detailed seeing surprising inconsistencies in how information moved in and out memory. There is research [67] in progress to limit tunneling by electrons through narrow materials. Gate tunneling was a key explanation behind the presentation of high-k dielectric materials [12]. This property allows them to be comparable to an ideal proportionate oxide thickness. In any case, at advanced nodes, that is absurd since gate oxides decrease with the rest of the other transistor features.

Venturing into the field of quantum physics, quantum effects are to a great extent a component of the dual nature of electrons, both as particles and as waves. Quantum effects in the field of physics include:

- scattering effects
- volume inversion
- Surface inversion

At the point when we start discussing narrow FinFET gadgets or even nanowires, rather than having surface inversion, suddenly the gadget is completely depleted. Depletion effect is caused by geometrical confinement [47]. In this paper, interest is on the germanium based FinFET and Vimala and Kumar [67] state that, "Quantum effects arise due to the confinement of moving electrons in the Ge film". Quantum confinement has a couple of different consequences. Among them:

- change in threshold voltage
- density of states (DOS) change
- carrier injection velocity change

DOS means the number of carriers ready for the ongoing conduction. The transistor threshold voltage change can be promptly remedied with process technology. Be that as it may, changes in the DOS and the carrier injection velocity lead to changes of the drive current changes in the gadget. Study of the movement of electrons in the Ge-film has shown that electrons move randomly but restricted in specified energy levels in quantum wells [47]. The fundamental quantum mechanical effects limitations to scaling include;

- quantum mechanical tunnelling
- Band to Band tunnelling
- direct gate oxide tunnelling
- source-drain tunnelling

Quantum mechanical tunnelling is a standout quantum mechanical effect where the electrons tend to move through a hindrance or a barrier that they classically shouldn't almost certainly travel through [12]. Classical term here emphasizing that these subatomic particles are not supposed to cross through the barrier unless if

they have ample potential energy to do so. This is in accordance to the laws of classical mechanics. These effect fully shows that the depletion layer widths should indeed always be bigger than the transistor channel width ($> 5nm$) otherwise tunnelling current will arise [67]. The situation where we experience tunnelling current is when there is a negative depletion layer.

There is study in progress to limit tunneling by electrons through narrow materials. One such methodology is a spin lattice done utilizing spin transfer torque (STT), which can restrict or "contain" the random electrons.

2.3 Multi-Gated MOSFET

The need for increase in operating speed by the industry led to the evolution of many ways to overcome SCEs while on the hand increasing current drive. This has lead to the shift of focus from classical single-gate transistor structures to multiple-gate MOSFET architectures [8]. On top of SCEs, planar MOSFET also have poor gate control [21]. Multi-gated MOSFET devices include double gate (DG), tri-gate (TG) and gate all around (GAA) [70]. The tri gate MOSFET standout amongst the three and it's the most reassuring structure for CMOS scaling to nanometer magnitude because of its capacity to hold back SCEs. However silicon based TG MOSFET just like the planner silicon based MOSFET also experiences scaling and performance limitations. The main ultimate limitation to the scaling of transistors is the atomic structure [43] of matter. A MOSFET cannot be smaller than an atom. Furthermore, with vigorous downscaling, lets say in the nanometer regime, quantum mechanical effects become prominent [44]. Standout quantum mechanical effect is tunnelling [71], where the electrons tend to travel through a hindrance or a barrier that they classically shouldn't almost certainly travel through. These effect fully shows that the depletion layer widths should indeed always be greater than the transistor channel width otherwise there will be a negative depletion layer leading to the flow of tunnelling current. To be specific, below 5 nm, one can encounter quantum mechanical tunnelling [45].

2.3.1 FinFET

Transistors are categorized into two categories: two dimensional and non-planar, which include multi-gate transistors such as FinFET. Conducting channels are present on all three sides of the vertical fin in TG transistors. FinFET and other multi-gate transistors use a single gate placed on top of two vertical gates, enabling electrons

to move freely across nearly three times the surface area. FinFET have less leakage while using less energy than two-dimensional transistors. The supplemental gate control allows much more transistor current to flow as possible whenever the transistor is in the ON-state (for effectiveness) and close to zero whenever the transistor is in the OFF-state (to reduce power), and allows the transistor to toggle between the two states incredibly fast [77] [50]. Non-planar MOSFET also offer positives in terms of packing density, carrier transport, and device scalability. DG and GAA MOSFETs have been studied for for a period of time, but because of their complex fabrication process, they were not seriously considered by the industry. Because of many scaling limitations related with planar (two-dimensional) CMOS, these structures have resurfaced in deep-sub-0.1 μm CMOS. Despite the fact that a number of device structures have been developed in the past, the market's attention has been drawn to FinFET, a DG device suggested in 1999 [78] because of its quasi-planar structure and comparatively straightforward fabrication. Originally, the gadget was known as a folded-channel FET [79].

Fin field-effect transistor (FinFET) is a summed up term utilized for any gadgets utilizing silicon fin as body built over an oxide substrate. Fundamentally GAA cannot be categorized as a FinFET while TG MOSFET is one of the FinFET implementations. A progressively proper term would be TG FinFET since lately MOSFET is popularly associated with non SOI structures like bulk MOSFET. FinFET technology is highly recommended as an alternative for CMOS to suppress limitations brought forth by the vigorous downscaling [22] since a better gate control is guaranteed [45]. Performance of superior quality and incorporation of VLSI have been bolstered by the scaling of Si MOSFET. Nonetheless, performance enhancement has been troublesome on account of the limits of Si MOSFET more especially, the physical ones.

2.3.2 History of Multi-Gated Structures

SOI MOS transistors have progressed from traditional, 2D, single-gate devices to 3D devices with a multi-gate structure (double gate, triple gate or quadruple gate) in an ongoing aim to bolster current drive. It is fair to say that the phrase "double gate" usually refers to a single gate electrode that is available on two opposite ends. Likewise, the phrase "triple gate" refers to a single gate electrode which is folded across three sides of a transistor. The MIGFET (Multiple Independent Gate FET) is a notable exception, as two distinct gate electrodes are being biased with varying potentials. SOI MOSFET are evolving from single-gate, partially depleted devices to multi-gate, completely depleted structures. Partially depleted silicon MOSFETs

are the direct descendants of early Silicon-On-Sapphire (SOS) devices. Partially depleted SOI MOSFET were first used in specialized applications like radiation-hardened as well as high-temperature electronics. Partially depleted SOI technology became common place around the turn of the century, when big semiconductor manufacturers began to use it to produce high-performance microcontrollers. The low-voltage performance of partially depleted SOI devices could be improved by making a connection between the gate electrode and the device's floating body. This type of contact enhances the subthreshold slope, body factor, and current drive, but it restricts the device's function to deliver voltages less than one volt. Electrostatic coupling between the gate and the channel is improved in Depleted Silicon Substrate devices [62, 80–83]. As a result, the linearity, subthreshold slope, body coefficient, and current drive are improved. Depleted Silicon Substrate technology, also known as Fully depleted SOI, is used in a variety of applications from low-voltage, low-power to RF integrated circuits.

[84] presented the first article on the DG-MOSFET in 1984. These devices continued to improve as a result of the need to raise threshold voltage and improve the current drive. The MIGFET (Multiple Independent Gate FET) is a DG device wherein the two gate electrodes aren't really linked and thus can be biased with different voltages. The key feature of the MIGFET is that bias applied to one of the gates modulates the V_{TH} of the other gate. [85–88]. The triple gate MOSFET, on the other hand, is a thin-film, narrow silicon island with gates on three sides. The quantum-wire SOI MOSFET [89, 90] and the TG MOSFET are two examples of implementations [91].

2.4 Germanium

In the past, germanium was surpassed by silicon as the preferred semiconductor for profit-oriented CMOS technology. However, the market quickly reached a limit when it comes to how small silicon transistors could be manufactured, endangering future advances. The plan is to substitute silicon with an element capable of moving current at higher rates. Fabricating transistors with these kind of channels might enable designers to keep on making speedier and more energy-efficient circuits, resulting in improved computing devices and smartphones. Germanium is one element being viewed as a possible replacement for silicon since it could allow the industry to produce smaller transistors and more compact ICs. As it was stated in section 2.2.1, it's hard to improve performance due to limits of Si MOSFET, more specially the physical ones. Researchers [67] [42] saw the need to overcome this,

and this opened doors to new materials used as alternatives to silicon. Germanium has caught an eye lately as a prospective channel contender for future MOSFET [92].

For an a while, the buzz around alternate channels was focused on III-V materials like gallium arsenide, which are made from atoms in the periodic table's columns just to the left and right of silicon. The III-V approach, however, was eventually discovered to have some essential physical limitations. Furthermore, it is highly probable to be prohibitively costly and hard to easily integrate with present silicon technology.

2.4.1 Ge vs Si

Experiments such as [67] have been carried out and different models have been used to prove that indeed germanium can yield much better results in terms of performance and efficiency enhancement for CMOS mitigated devices. Germanium has high channel mobility while on the other hand Si Tri gate MOSFET has higher electron and hole mobility [67]. Germanium has the solid potential for diversifying the applications of CMOS circuits. Attributes that makes germanium to highly promise to be a possibility for silicon channel replacement for future advanced CMOS innovations include:

- Straightforward and silicon compatible fabrication process
- Flexibility with germanium oxynitride (GeON), high dielectric constant and metal gate
- High carrier mobility over silicon
- High hole mobility, almost 2 times enhancement over Si
- High channel mobility, for instance Ge TG-MOSFET has higher channel mobility when compared to Si TG-MOSFET [67]

For Ge bulk MOSFET, the p-channel has an edge over the n-channel, to be specific, n-channel has a drive current of one to two orders of magnitude lower [39].

It is clear the problem with Si MOSFET is to maintain performance of superior quality when the geometries of a transistor are varied but without losing current and threshold potential on the process(trade-offs). Germanium is regularly utilised for high performing devices as an alternative to silicon. Very low threshold potential which is the source for fast turning-on of devices is a standout setback for this device

[42]. This major setback eventually also leads to high SCEs which will result in high delay time, thus diminishing the switching speed. For Ge based devices, quantum confinement effects such as quantum-confined Stark effect (QCSE) always arise [46]. Quantum effects arise due to the confinement of moving electrons in the Ge film. Study of the movement of electrons in the Ge-film has shown that electrons move randomly but restricted in specified energy levels in quantum wells [47]. In this way an analytical model is required to plan future integrated circuits (IC). This research deals with developing a model that allows a Ge FinFET to operate at a low threshold voltage efficiently without many trade-offs in terms of leakages and tunnelling. The research can also give an excellent platform to study and overview the quantum effects in a FinFET. The device performance made of germanium material can be compared to the previous devices made of silicon material and how a germanium based device can be further improved for CPU switch applications.

2.5 Related Works

Sekigawa and Hayashi 1984 [84] was the first ever article on DG MOS transistor published [12]. That paper shows that one can get critical decrease of SCEs by sandwiching a completely depleted SOI gadget between two gate terminals associated together. The gadget was called XMOS in light of the fact that its cross area resembles the Greek letter Ξ . Utilizing this arrangement, Agrawal [93] got a superior control of the channel depletion area than in an "ordinary" SOI MOSFET, and, specifically, the impact of the drain electric field on the channel is decreased, which lessens short-channel. Table 2.3 shows migration of scaling of MOS structures and what influenced certain innovations.

TABLE 2.3: Migration of scaling of FET and how technology evolved overtime

Article or Paper	Title	Brief description	Limitations
1. Sekigawa and Hayashi [84]	Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate.	Squeezing a fully depleted SOI device in-between gate electrodes that are connected to reduce SCEs.	Higher power with processing power unable to meet the ever increasing demand. There was still work to do to improve the design of the device but it is understandable as this was the first device ever presented [12].
2. Agrawal et al [93]	Short channel models and scaling limits of SOI and bulk MOSFET.	The channel depletion region control is better than in the traditional SOI MOSFET. Reduction of influence of the drain electric field on the channel, which decreases short channel. The minimum acceptable channel lengths are calculated from the criterion that V_{TH} and subthreshold swing (S) must not degrade beyond the point where the I_{ON}/I_{OFF} falls below two decades.	As time passes, the demand for processing power increases which means the device was overdue before long.
3. Frank, Laux and Fischetti [94]	Monte Carlo simulation of a 30 nm dual-gate MOSFET: how short can Si go?	The first project to study scaling of Si-MOSFET. The ultimate Si device is a DG SOI MOSFET with $L_G = 30$ nm, $t_{OX} = 3$ nm and Si film thickness of 5 nm - 20 nm. Simulation results showed no SCE for $L_G > 70$ nm and $g_m \leq 2300$ mS/mm.	The simulation results show that if $L_G > 70$ nm, there are no SCE. The Si L_G in this case is 30 nm, implying that SCE may exist.

Article or Paper	Title	Brief description	Limitations
4. Hisamoto et al [95]	A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET.	The first DG SOI MOSFET to be fabricated. The DELTA MOSFET designed in a similar manner as the FinFET. The difference is that the FinFET include a dielectric layer named the “hard mask” on top of the Si fin.	Formation of parasitic inversion channels at the top corners of the device, the dielectric layer in the FinFET is used to prevent this [78] [12]. This is the main reason why DELTA MOSFET didn’t get a proper breakthrough.

Article or Paper	Title	Brief description	Limitations
5. Onai et al [96]	0.1 μm CMOS technology for high-speed logic and system LSIs with SiO/SiN/poly-Si/W gate-system.	SiO/SiN stacked gate dielectric with $t_{OX_{inv}} = 2.8 \text{ nm}$ to prevent direct tunnelling leakage and boron penetration. Reduction of gate resistance by usage of a poly/metal stacked gate electrode. Short channel working at a supply of 1.5 V for $L_G < 0.1 \mu\text{m}$ and drive currents of $1000 \mu\text{A}/\mu\text{m}$ and $1410 \mu\text{A}/\mu\text{M}$ for NMOS and PMOS respectively.	It is critical to develop technologies for finer patterning and other new process-related technologies in order to make systems more effective, power-efficient, and smaller in order to manufacture systems-on-a-chip for an ever-growing variety of multimedia and mobile communication applications. The effect of the V_D on the I_D is still significant at $L_G \approx 0.1 \mu\text{m}$, resulting in higher DIBL [97].

Article or Paper	Title	Brief description	Limitations
6. Bin Yu et al [98]	FinFET scaling to 10 nm gate length.	In the year 2002, this was the smallest DG transistors ever made. A design with $L_G = 10$ nm and fin width scaled down to 12 nm. The was the best ever performing transistor reported by the time concerning short channel behaviour. The FinFET outperformed the traditional planar Si-MOSFET. Huge improvements in the channel crystal orientation and hole mobility in general. Better gate control guaranteed.	Issues like parasitics reduction and the engineering behind the gate material.
7. Chang et al [99]	Extremely scaled silicon nano-CMOS devices.	Usage of lightly doped material, gate work function be tunable for 4.4 eV - 5.0 eV to give a means for adjusting the device V_{TH} . Selectively adjusting to achieve multiple V_{TH} values which will allow optimization of high-performance against low-power applications in the absence of channel doping. SCEs reduced when the body thickness is 4 times smaller than the gate length ($T_{fin} = \frac{1}{4}L_G$). Sublime drive current can be attained with a comparatively thick gate oxide ($t_{OX} = 2.1$ nm), with resistance restricted to low values by thickening the contact regions.	Although the potential benefits of metal gate electrodes important, the challenge of metal selection and process integration will almost certainly necessitate significant research and development efforts in the coming years.

Article or Paper	Title	Brief description	Limitations
8. Collaert et al [100]	A functional 41-stage ring oscillator using scaled FinFET devices with 25 nm gate lengths and 10 nm fin widths applicable for the 45-nm CMOS node.	A functional FinFET ring oscillator ($V_{TH} = 0.2$ V) with a physical gate length, $L_G = 25$ nm and a fin width of 10 nm, the smallest ever reported at the time of publication. A tall and narrow ($W_{subfin} = 10$ nm and $H_{subfin} = 60 - 80$ nm) fins are needed to suppress SCEs which leads to drain-induced barrier leakage features of 45 mV/V at $V_{DD} = 1$ V and $L_{subg} = 25$ nm.	In this project, metal gates weren't used. Although polysilicon was used to address the issue of metal gates rising V_{TH} , the same material when doped at practical levels doesn't provide the near-zero electrical resistance given by metals, and is therefore not ideal for charging and discharging the gate capacitance of the transistor.
9. Shang et al [101]	Germanium channel MOSFETs: Opportunities and challenges.	Surface passivation and gate dielectric, dopant diffusion, and junction leakage are the leading challenges related to germanium CMOS gadgets. Integration with less processing challenges, notably high hole mobility, and enhanced electron mobility. There is still room for work that has to be done in the ultra-modern short channel germanium MOSFET with adequate performance upgrade.	The article states both the opportunities and challenges, therefore another model has to be developed in order to address the challenges.

2.6 Chapter Summary

MOSFET, a semiconductor structure, is scalable, which means that a large number of them can be manufactured in a single wafer. Semiconductors are materials that, depending on the conditions, can function as either an electrical insulator or a conductor. This conduct is caused by two electrical properties: the bonding properties of the individual atoms that make up a bulk material and the interactions of their external electrons. An atom's central nucleus is made up of protons and neutrons, and it is surrounded by an electron cloud. This electron cloud is made up of quantized shells with varying energies. Each electron in this circling cloud must maintain a quantized energy level. Each rigid material is made up of individual atoms that are coordinated in a specific way and can be classified as amorphous, crystalline, or poly-crystalline depending on the atom arrangement. Electrons are limited to occupying energy bands in a solid because they can only exist at specific quantized energy levels in an individual atom. Each of these energy bands contains a range of energy levels that each electron can occupy. The valence and conduction bands are the only energy bands of significant concern in MOS applications. The band-gap of a material determines and influences its ability to conduct electricity. The band-gap in insulators is relatively large, and it takes a large amount of energy to excite free electrons. Semiconductors, on the other hand, have a relatively small band-gap, allowing them to function as insulators or conductors depending on the energy level of the material. When bonds in a material are broken as a result of energy absorption, two types of charge carriers called electrons and holes are formed. Doping is the process of deliberately introducing impurities into a semiconductor material in order to control its electrical properties. A completely undoped semiconductor is referred to as intrinsic, whereas a doped semiconductor is referred to as extrinsic. Doping a semiconductor with either p-type or n-type material is possible. The majority of semiconductor applications, including FET, are conceivable due to the properties formed by the intersection of a p-type region and an n-type region, resulting in a p-n junction that functions as a diode. Due to the limitations of traditional planar MOSFET scaling, performance enhancement has been difficult, leading to the gradual evolution of the SOI MOSFET from partially depleted, single-gate devices to multi-gate, fully depleted structures. Scaling issues include SCEs and QMEs. FinFET is a catch-all term for any device that has a silicon fin as its body and is built on an oxide substrate. The technology is highly recommended as an alternative to CMOS for suppressing limitations caused by intense downscaling.

Chapter 3

Theory of Field-Effect Transistors

In this section, reference will be made to a standard n-type depletion mode MOSFET (Figure 3.1). The basic operation of a MOSFET was stated earlier in Chapter 2. Other than the depletion mode MOSFET, there is also the enhancement mode MOSFET. The device has two consecutive p-n junctions combined forming a channel between them. The source/drain blocks regularly have high doping contrasted with a generally low doped p-type substrate. A n-channel is formed even before a positive bias is connected to gate electrode which is disengaged from it by any material which does not conduct electricity. MOSFET source/drain are typically exceedingly doped for ohmic contacts.

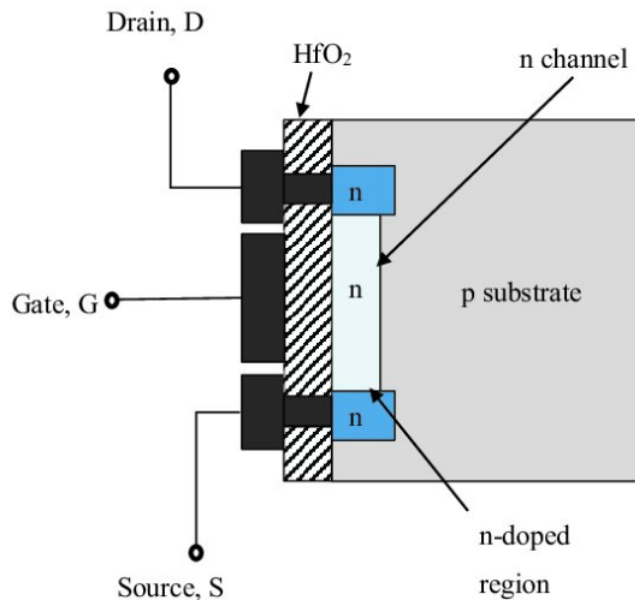


FIGURE 3.1: n-type depletion mode MOSFET

The source and drain leads are each connected to the two n-doped regions and this regions are linked by a n-channel. Also these n-doped regions lies on a p-doped substrate. The gate connect to this channel through a thin layer which acts as an insulator and this layer is usually an oxide, hafnia (HfO_2) or silica (SiO_2), or high- k dielectric material.

3.1 Energy Band Diagrams

Considering a n-type MOS diode with its energy band diagram at thermal equilibrium. For this discussion, the primary center will be a ideal device equipped with all the essential material, for example, oxide insulator and silicon bulk substrate. At thermal equilibrium, it is expected that the channel is consistently doped and there is no charge in the oxide layer. The energy difference between the metal work function $q\Phi_m$ and the semiconductor work function $q\Phi_s$ is zero in this ideal case (see Equation 3.1) and furthermore the vacuum level is high to such an extent that carriers can't surmount the potential barrier. The horizontal energy band in the insulation layer induces that there is no applied bias across the gadget [102–104]. The following condition is derived from thermal equilibrium state.

$$q\Phi_{ms} \equiv (q\Phi_m - q\Phi_s) = q\Phi_m(q\chi + \frac{E_g}{2} + q\Phi_B = 0 \quad (3.1)$$

where $q\Phi_m$ and $q\Phi_s$ are metal work function and the semiconductor work function respectively. Other symbols are described below.

- E_c - conduction band energy level
- E_f - Fermi level energy
- E_v - valence band energy level
- E_g - band gap
- $q\chi$ - electron affinity

Electron affinity is the gap between the vacuum and conduction level energy.

At the point when a little negative voltage ($V < 0$) is connected at the metal, the energy bands close to semiconductor surface are twisted downward and the electrons, which in this case are the majority carriers, are depleted near the surface. The gate will have a negative charge (Q_m) and a correlating charge in the semiconductor will be $Q_{sc} = qN_D W$ [102–104].

From depletion mode, a perfect MOS diode function changes to inversion mode when a bigger negative voltage is connected. At this stage, the downward bending of the energy bands will be of greater degree causing the intrinsic level (E_i) at the semiconductor surface to traverse Fermi level [104]. At the point when this occurs, excess holes are actuated at the substrate-insulator interface expressed by charge per unit area Q_p . Along with with charge per unit area Q_{sc} and the bending of the

surface band given by $\Phi = 2\Phi_B$ [105] [106] [107], the all out semiconductor charge is:

$$Q_s = Q_m + Q_{sc} = Q_p - qN_D W_m \approx \sqrt{2\epsilon_{ZnO}\epsilon_0 q N_D \phi} \quad (3.2)$$

W denotes depletion width while the doping concentration in the bulk substrate is expressed as N_D .

The concentration of electrons is determined by the gap between the Fermi level (E_f) and the intrinsic level (E_i). The concentration and the energy difference are exponentially related whereby for an n-type $E_f - E_i$ is used and $E_i - E_f$ for p-type [102–104]. The relationship is clearly shown in Equation 3.3.

$$n_p \approx n_i e^{-\frac{E_i - E_f}{kT}} \quad (3.3)$$

3.2 Work Function Difference

Although theoretical the MOS diode is taken as it have ideal features, in real life its work-function doesn't equate to zero (see Equation 3.4). These is due to the fact that the material used in the semiconductor is not the same material used for the electrode.

$$q\Phi_{ms} = q\Phi_m - q\Phi_s \neq 0 \quad (3.4)$$

For the device to remain switched-on, the work function should be equivalent to a larger value as this promotes the continuous flow of current. As it was stated earlier, the work-function in ideal situations is equivalent to zero which is a very desired case. The trapped charges just like the workfunction difference are undesirable defects. This include:

- Oxide fixed (Q_f)
- Interface state (Q_{IT})
- Oxide trapped charge (Q_{ot})
- Mobile oxide charge (Q_m)

Both oxide trapped charge and the mobile oxide charge are neglected most of time(see Equation 3.5) as they don't have more prominent impact as the other two charges (interface state and oxide fixed trapped charges) [102–104, 108, 109].

$$V_{FB} \approx \Phi_{ms} - \frac{Q_f + Q_{IT}}{C_{ox}} \approx \Phi_{ms} - \frac{Q_{IT}}{C_{ox}} \quad (3.5)$$

C_{ox} being the oxide capacitance while Q_{ms} denotes the difference in voltage calculated in reference to the metal and the semiconductor.

3.3 MOSFET Drain Current Equations

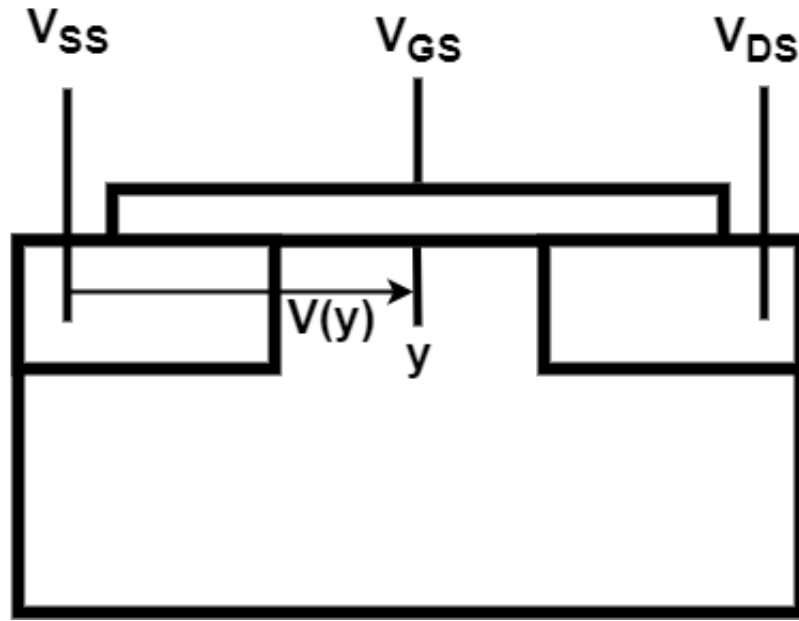


FIGURE 3.2: Movement of carriers in a uniform narrow channel

The study will mainly focus linear (see Figure 3.2) region to derive linear equations of the MOSFET. For a transistor to operate in linear region, gate-source voltage (V_{GS}) has to be greater than threshold voltage (V_{TH}) otherwise diffusion current will be more pronounced. A field effect transistor consists of a pair of drain current (I_D) and diffusion current combined together. As it was stated earlier, for derivation of MOSFET linear equations, the transistor is considered to be operating in linear region thus the I_D should be prominent which means neglecting the diffusion current.

$$dV = \frac{I_D dy}{\mu_{FE} W |Q_{acc}(y)|} \quad (3.6)$$

$$Q_{acc}(y) = C_{ox} |V_{GS} - V_{TH} - V_y| \quad (3.7)$$

μ_{FE} denotes the field effect mobility while $Q_{acc}(y)$ represents total accumulated charge per unit area prompted at a point y inside the channel.

Rearranging Equation 3.6 we get

$$I_D dy = \mu_{FE} W | Q_{acc}(y) | dV \quad (3.8)$$

which can further be expanded (see Equation 3.9) by substituting Equation 3.7.

$$I_D \int_0^L dy = \mu_{FE} W \int_0^{V_D} [C_{ox}(V_{GS} - V_{TH} - V_{(y)})] dV \quad (3.9)$$

$$I_D = \frac{WC_{ox}\mu_{sat}}{L} [(V_G - V_{TH})V_D - \frac{V_D^2}{2}] \quad (3.10)$$

The condition $V_D \ll V_{GS} - V_{TH}$ implies that the device operates in linear region, hence

$$I_D = \frac{W}{L} C_{ox} \mu_{FE} (V_{GS} - V_{TH}) V_D \quad (3.11)$$

In saturation region, drain bias does not impact current ($V_D > V_{GS} - V_{TH}$), hence

$$I_D = \frac{W}{2L} C_{ox} \mu_{sat} (V_G - V_{TH})^2 \quad (3.12)$$

3.4 Chapter Summary

A MOSFET is made up of two consecutive p-n junctions that form a channel between them. At thermal equilibrium, the channel should be consistently doped and the oxide layer should be free of charge. In this ideal case, the energy difference between the metal and the semiconductor work function is zero, and the vacuum level is high enough that carriers cannot overcome it. When a small negative voltage is applied to the gate, the energy bands near the semiconductor surface twist downward, and the electrons, which are the majority carriers in this case, are depleted near the surface. The gate will have a negative charge, and the semiconductor will have a corresponding charge of $Q_{sc} = qN_D W$. When a larger negative voltage is connected to a perfect MOS diode function, it transitions from depletion mode to inversion mode, indicating that the energy bands are more bent downward, causing the intrinsic level at the semiconductor surface to traverse Fermi. The gap between the Fermi level and the intrinsic level determines electron concentration. The concentration and the energy difference are exponentially related, with $E_f - E_i$ for

an n-type and $E_i - E_f$ for a p-type. Although the MOS diode has ideal features in theory, its work-function does not equate to zero in practice because the material used in the semiconductor is not the same material used for the electrode. A field effect transistor is made up of a pair of drain and diffusion currents combined.

Chapter 4

Design and Simulation

Design and simulation will aid in the verification and validation of the purpose of the germanium-based fin field-effect transistor under advancement, including the product's manufacturability. The term "simulation" is frequently used to refer to computer-aided engineering (CAE). Numerous design simulation approaches are increasingly becoming core features of product development throughout many industrial sectors, and their significance is growing as low-cost, quicker computers and low-cost, straightforward design simulation software enable people to resolve new technologies and applications. In our case, the simulation software used is Silvaco.

4.1 Methodology

The proposed plan of work was to develop a Ge based FinFET. The project ran for 24 months. Figure 4.1 shows the detailed steps followed in order to achieve the objectives of the project.



FIGURE 4.1: Methodology

4.1.1 Simulation

Theoretical data found in [12, 22, 67, 70, 78] gave the project the initial direction as previous works and suggested solutions were analysed. In this case materials proposed by recent researches were simulated using Silvaco software products. This research project predominantly centred around the following:

1. DevEdit

2. Athena

3. ATLAS

The plan of action utilized genuinely physical-based gadget simulation to foresee electrical attributes related with the predefined physical structure and bias conditions. The idea was to design a 30 nm Ge FinFet of either n-type or p-type. A 3D structure is the best display that can be created to examine channel orientation and fin orientation [42] of the gadget. Different features like germanium concentration effects, stress effect and diffusion were mostly incorporated in the early studies.

Different materials can be considered for the insulator or the oxide as it is commonly known, and the gate (see Figure 2.1). In a traditional MOSFET, polysilicon is commonly used for the gate. Kong et al [110] investigated the impact of grain size in polysilicon and how it influences the gate leakage. The study show that bigger grain sizes claims high interface roughness due to grain protrusion into the layer of the gate oxide during post annealing, which will decrease the oxide thickness effectiveness (t_{OXeff}) leading to failure or malfunction of the gate oxide. Rather than polysilicon, metals on the other hand when doped at practical levels give near-zero resistance which is ideal for charging and discharging the gate capacitance. Based on the literature [12, 102, 104], simulation results from [67] and the fact that germanium naturally has low threshold voltage when compared to silicon [42], polysilicon was selected for the gate. Polysilicon has almost the same chemical composition as the bulk-Si channel, which means it is also similar to the Ge channel. Furthermore, because polysilicon is a semiconductor, the work function can be modulated by changing the doping level. Material selection and simulation details is elaborated more in Section 4.2 and Section 4.2.3 respectively.

4.1.2 Numerical Modelling

Numerical methods are needed in order to come up with models. Two ATLAS numerical methods namely Newton and Direct were used. The Newton strategy explains the all out arrangement of unknowns together. It is valuable when the arrangement of equations is heavily coupled and has quadratic convergence. It might invest additional energy solving for amounts that are basically consistent or weekly coupled. Anyway for practically cases, this strategy is mostly used and it is the default one.

The Gummel technique comprehends for every unknown thus, keeping different factors steady and repeating the procedure until a stable solution is accomplished.

This technique endures moderately poor initial guesses. For the most part, it is helpful where the system of conditions is weakly coupled however has just linear convergence. Its only limitations are lumped components or current boundary conditions and it is important to note that the method is very slow to use.

On top of Newton and Gummel methods, there is also the Block method but unfortunately the latter cannot be used in 3D simulations.

A couple of researchers [111–114] have modeled SCEs in silicon-on-insulator metal-oxide semiconductor field-effect transistors by either one between the two of charge sharing analysis and working out the two dimensional Poisson equation existing in the channel domain. For $L_C < 1 \mu\text{m}$ (which includes our case), the models of charge sharing become incorrect. An analytical model for short channel V_{TH} which was two dimensional, was brought fourth by working out the Poisson equation in a completely depleted narrow layer silicon-on-insulator metal-oxide semiconductor field-effect transistors thanks to [114]. Physical insights into the dependence of SCEs on system parameters were obscured due to the solution's complexity. As a result, in completely depleted short channel silicon-on-insulator metal-oxide semiconductor field-effect transistors, Agrawal [93] came up with a two-dimensional analytical model for V_{TH} , S , and sub-threshold drain current.

Electric potential of germanium which is very helpful as it based on germanium film thickness, can be solved with the use of Schrödinger–Poisson equation. Ge film thickness can be developed by Quantization due to quantum effects [67]. Section 4.2.1, the model for this research project, is based on a quantum mechanical variational approach which depends on the Schrödinger–Poisson equation. The presentation of Schrödinger–Poisson equation is on Section 4.2.1.

4.1.3 Comparative Analysis

Comparative analysis is based on extensive simulation framework using Silvaco software products and it is where parameter optimization is mostly centered. Simulation trials are compared to see trends and where each increase or decrease in a parameter value leads. The parameters that are varied include doping concentration, fixed charge (qf), nc300, and nv300. It yields results which lead to selection, as a better and effective design is determined here. Systematical investigation is presented using I-V characteristics to demonstrate the sensitivity or how critical design parameters of Ge FinFET are to the device's figure of merits. Investigation is

done through C-V curves and I-V characteristics to study parameters and electrical properties such as:

- Threshold voltage
- Charge carrier density
- On and Off current ratio
- DIBL
- Subthreshold Swing
- Carrier concentration
- Conductance

4.1.4 Selection

The 30 nm Ge FinFET is designed by parameter optimization which is achieved through investigation of multiple design parameters and assessing their effects. Parameters are maximized and minimized to see how they affect the overall operation of the device, and with the help of control parameters such as On/Off current ratio ($I_{On/Off}$) and threshold voltage (V_{TH}), optimal parameter values can be found but not minimum and maximum. The aim is to have the device performing efficiently regarding power and processing speed but without a lot of trade-offs. Design parameters are set based on comparative results, Section 4.1.3.

The fin dimensions influence the electrical parameters of the transistors such as drive current and threshold voltage. Variations in dimensions has to be done carefully to avoid trade offs though. Material specifications used are stated on Table 4.1 and selection was based on compatibility and performance with aid from related works [22, 67, 70]. Methods mostly used to extract semiconductor materials include Spray Pyrolysis and Hydrothermal Synthesis. Spray Pyrolysis is a depositing of thin films of a certain material onto glass substrates [115]. Hydrothermal synthesis is a single-crystal synthesis process that takes advantage of mineral solubility in hot water under high pressure. The crystal growth takes place in an autoclave, which is a steel pressure vessel that is supplied with both a nutrient and water.

4.2 30 nm FinFET Modelling and Design

This research is concerned with the design of a 30 nm Ge based Tri-gate (TG) MOSFET. TG is more scalable than the double gate (DG) [116]. A gate electrode is used to wrap a thin Ge body with dimensions thickness (t_{fin}) and height (H_{fin}). A channel with length (L_G) is formed between the source and drain. H_{fin} is half the effective channel length while t_{fin} (also denoted W_{top}) is almost a quarter of the L_G . Gate length and channel length are interchangeable, although they are not really equal. After doping by implantation and self-aligned process, the n^+ regions extend a little bit under the gate because of the side diffusion of the implanted ions (see Figure 4.2).

$$L_C = L_G - 2L_D \quad (4.1)$$

The L_D in Equation 4.1 denotes the diffusion length, which is a very small value. The effective channel length would then be the actual distance a carrier covers from source to drain. As it was stated, the diffusion length is very small ($L_D \approx 0$) hence channel length (see Equation 4.1) is taken as the gate length ($L_G \approx L_C$), although mathematically, the channel length is a little bit smaller ($L_C < L_G$).

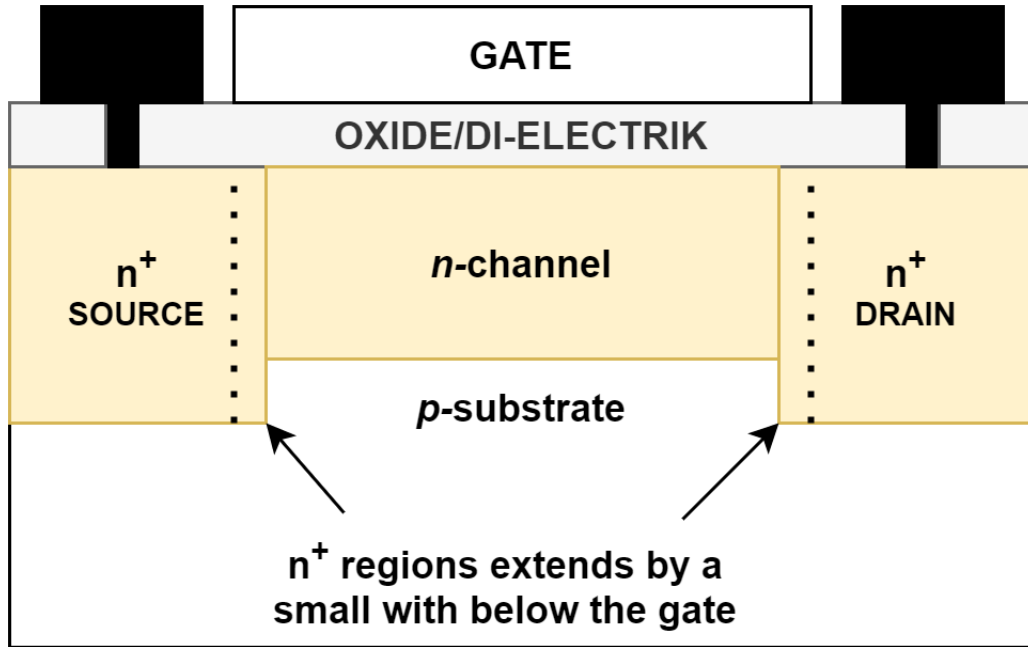


FIGURE 4.2: Diffusion of implanted ions shown in a MOSFET structure

A gate oxide with thickness (t_{OX}) is used to separate the gate electrode and the channel. [117] and [42] are both used in this work as reference regarding the device model and other device specifications such as doping.

TABLE 4.1: Ge FinFET material specifications

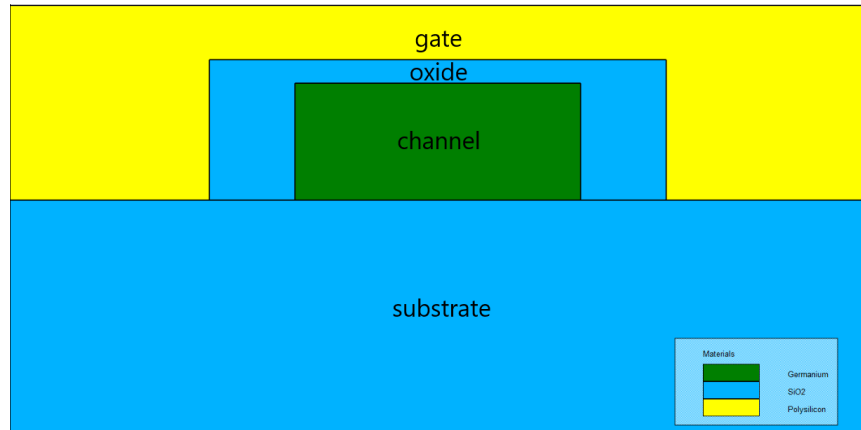
Device material specifications		
Region	Material	Simulation Pattern
Gate	PolySilicon	0x5
Oxide	Silicon Oxide	0x2
Channel	Germanium	0x4
Source	Aluminium	0x7
Drain	Aluminium	0x7
Substrate	Silicon Oxide	0x2

TABLE 4.2: List of design parameters

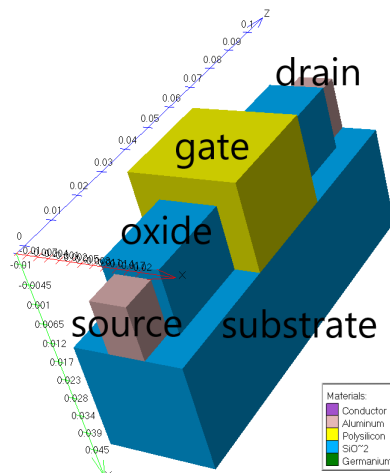
Device design parameters		
Parameters	Fixed Value	Range
L_G	30 nm	-
H_{fin}	15 nm	-
Fin width/thickness, t_{Ge} (t_{fin})	7.5 nm	-
Doping Concentration	1×10^{18}	$4 \times 10^{17} - 3 \times 10^{19}$
Intrinsic Carrier Concentration, ni	$2.4 \times 10^{13} / cm^3$	-
Effective mass of electrons, m_x	$1.64m_0$	-
Gate Workfunction, ϕ	4.85	-
nc300 = nv300	2.8×10^{19}	$4 \times 10^{18} - 8 \times 10^{20}$
Fixed Charge, qf	3.5×10^{12}	$1 \times 10^{11} - 5 \times 10^{12}$

TABLE 4.3: The affinity and permittivity values of respective regions within the device

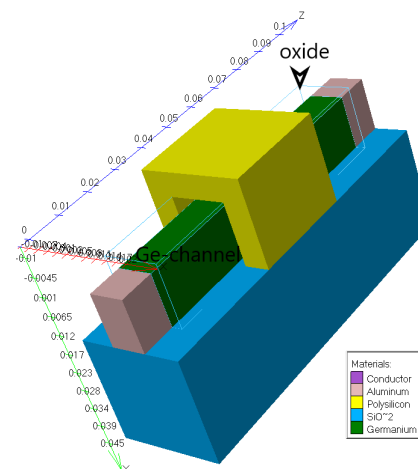
Affinity and Permittivity		
Region	Permittivity, ϵ	Affinity, E_{ea}
Channel	16.2	4.0
Oxide	3.9	1.0
Gate	11.9	4.05



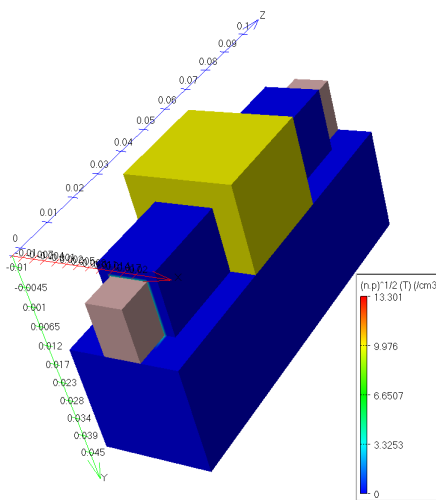
(A) Cross sectional area of a Ge-FinFET



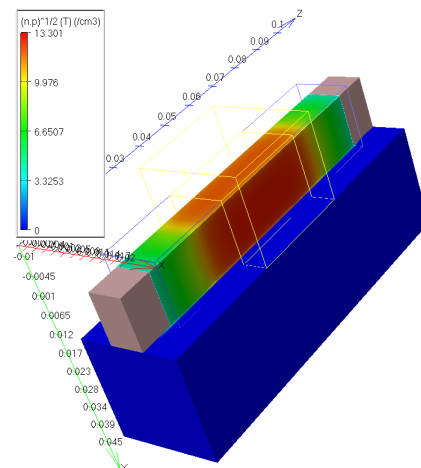
(B) Materials used for each section



(C) Channel Region



(D) Electron concentration for each section



(E) Electron concentration of the channel

FIGURE 4.3: Structure of the Ge FinFET

Table 4.1 shows a list of material used for each region. Table 4.2 show the dimensions and other design parameters while Table 4.3 shows the list of permittivity and affinity. Doping concentration, nc_{300} , and nv_{300} are design parameters that are optimized, and the fixed value is the optimal value in this case, despite the fact that nc_{300} is equal to nv_{300} , which means that only one of them can be presented.

Figure 4.3 shows the structure of the Ge FinFET including the materials used and the electron density of each region. Figure 4.3a and Figure 4.3d display the cross-sectional area and electron concentration throughout the device respectively. The Ge channel is clearly shown in Figure 4.3c and its channel concentration on Figure 4.3e.

4.2.1 Quantum Model

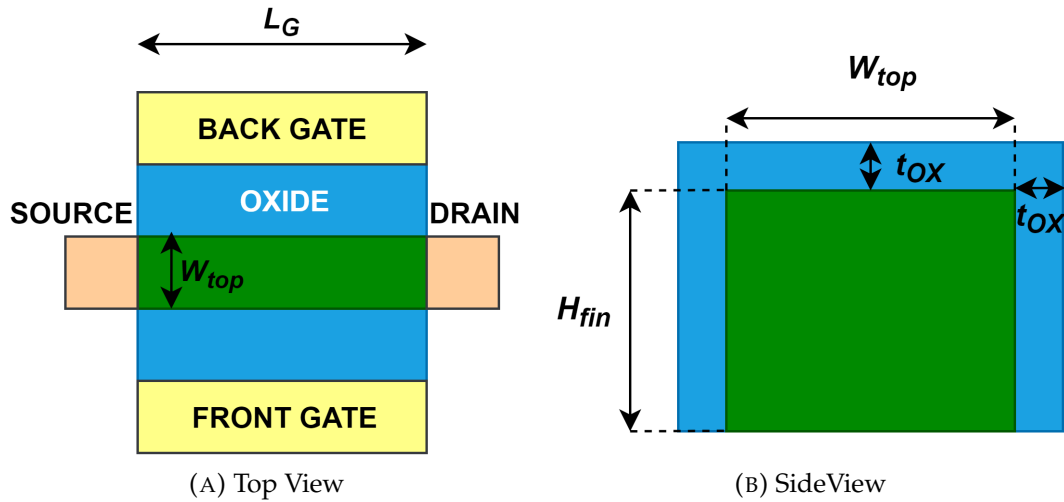


FIGURE 4.4: Cross sectional area of a DG Ge-FinFET

Figure 4.4 shows the cross-sectional area (both the side view and top view) of the structure of the Ge FinFET. An assumption made is that the motion of the electrons is only in a single direction, in the case of the Fermi potential defining the surface potential through some point x, y along the channel, its y -direction, and $imref$ (also known as a quasi Fermi level, and that is "imref" spelled forward) remains constant over the channel in the other direction, in this case, the x -direction [118].

Although this research project presents a TG design, a double gate (DG) can be used to study the quantum confinement effects. Unlike in bulk MOSFETs, where quantum confinement is caused by the surface potential [70], quantum effects in TG MOSFET are caused by the confinement of electron movement in the slim channel [12], which in our case is the Ge film. This is also true for DG MOSFET [70], which is

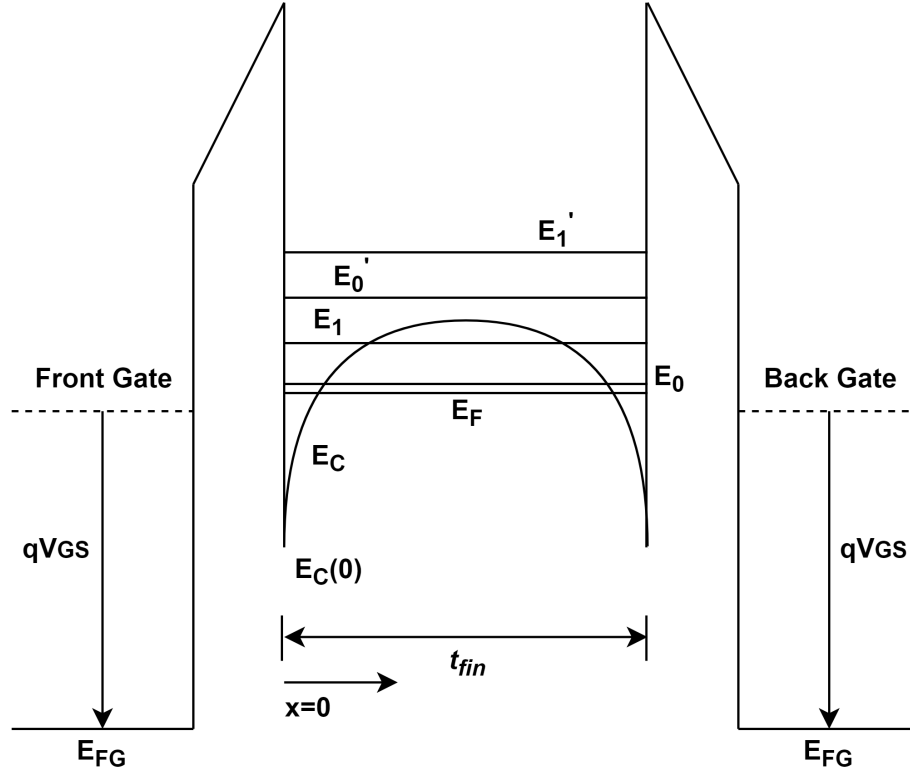


FIGURE 4.5: Energy-band diagram

why they are being used in this research project to study quantum confinement effects. Confinement can be viewed as the random movement of electrons constricted in certain energy levels in quantum wells and is influenced by the body thickness. Figure 4.5 shows a schematic energy-band diagram over the thin Ge channel of a symmetrical DG n-MOSFET with each gate supplied with $V_{GS} > 0$ as well as the quantised electron sub-band energies. The diagram is a vertical cross-sectional area which describes what is happening in the quantum well and the energy levels. The inversion charge carriers are also restricted within this well. To acquire the quantum attributes of DG MOSFET, the coupled Poisson–Schrodinger equation utilising the variational approach is adopted [70]. This equations are also an excellent platform to study how the wave function relates with the electron density [98]. Higher energy sub-bands are ignored and deemed less important because for smaller semiconductor thickness, at channel thickness less than 3 nm, only about 10% of electrons are not confined in the ground state of the lower sub-band [70] The confined inversion charge carriers are thickness dependent.

$$\frac{d^2\phi(x)}{dx^2} = \frac{q}{\epsilon_{Ge}} \left(N_A + N_{inv} |\psi_j(x)|^2 \right) \quad (4.2)$$

The non linear Poisson equation shown in Equation 4.2 is used to find the electrostatic potential. Originally, the Poisson equation is stated as [67] [70]

$$\frac{d^2\phi(x)}{dx^2} = \frac{q}{\epsilon_{Ge}} (N_A + n(x)) \quad (4.3)$$

where q denotes the charge, ϵ_{Ge} is the Ge permittivity, $\phi(x)$ is the surface or electric potential while $n(x)$ and N_A are electron density and acceptor concentration respectively. Equation 4.4 relates the electron density and the wave function ($\psi_j(x)$).

$$n(x) = |\psi_j(x)|^2 N_{inv} \quad (4.4)$$

Merging Equation 4.3 and Equation 4.4 results in Equation 4.2. The interface of the oxide and the semiconductor (where Ge channel meets the SiO₂) forces the conduction band to be divided into a couple of specified sub-bands due to the normal confinement of electron movement. With the use of $\phi(x)$ and the Eigen function $\psi_i(x)$ which in this context is determined for the lower energy sub-band E_i , variational approach can be used to come up with the Schrodinger equation (see Equation 4.5) for this sub-band [70]. This is achieved by integrating Equation 4.2 two times through $0 < x < t_{Ge}$ and using $\psi_j(x)$ as $\psi_0(x)$ for $j = 0$ which is the bottom energy sub-band eigenfunction.

$$\frac{-h^2}{8\pi^2 m_x} \frac{d^2\psi(x)}{dx^2} + (-q\phi(x)\psi_i(x)) = E_i \Psi_i(x) \quad (4.5)$$

Where h is the Plank's constant and m_x which is taken as $1.64m_0$ (see Table 4.2) is the effective mass of electrons in the x -direction.

Then the Eigen wave function could be expressed as

$$\Psi_i(x) = a_0 \sqrt{\frac{2}{H}} \sin\left(\frac{\pi x}{H}\right) \left[e^{\frac{-b_0 x}{H}} + e^{\frac{-b_0(H-x)}{H}} \right] \quad (4.6)$$

In this model, the variational approach is partnered with a trial wave function [56] (see Equation 4.7).

$$\psi_j(x) = a_j \left(\frac{2}{t_{Ge}} \right)^{\frac{1}{2}} \sin\left(\frac{(j+1)\pi x}{t_{Ge}}\right) \left(e^{\frac{-b_j x}{t_{Ge}}} + e^{\frac{-b_j(t_{Ge}-x)}{t_{Ge}}} \right), j = 0, 1, 2, 3, \dots \quad (4.7)$$

b_j and a_j denote variational parameter and normalisation constants respectively. Equation 4.8 shows the normalisation of Equation 4.2, $\int_0^{t_{Ge}} \psi_j^2 dx = 1$.

$$a_j = 2 \left(2e^{-b_j} + \frac{[(j+1)\pi]^2 (1 - e^{-2b_j})}{b_j [b_j^2 + ((j+1)\pi)^2]} \right)^{-\frac{1}{2}}, j = 0, 1, 2, 3... \quad (4.8)$$

b_j is found by $\frac{dE_j}{db_j} = 0$ reached from the quantum mechanical variational approach, hence by approximation, Equation 4.9 is the derivation of b_j where the depletion charge density, Q_d is given by $Q_d = qt_{Ge}N_A$ and the inversion charge density, Q_{inv} is found by $Q_{inv} = qN_{inv}$.

$$b_j = t_{Ge} \sqrt[3]{\frac{qm_x\pi^2 \left(Q_d + \frac{5}{6}Q_{inv} \right)}{\epsilon_{Ge}h^2(j+1)}}, j = 0, 1, 2, 3, ... \quad (4.9)$$

4.2.2 Drain Current

[67] developed a continuous analytical drain current expression for the modelled (section 4.2.1) inversion charge model for TG MOSFETs in this section.

$$I_D = \mu \frac{W}{L_C} \int_0^{V_{DS}} Q_{inv} dV \quad (4.10)$$

Equation 4.10 is obtained by,

$$I_D = \mu \frac{W}{L_C} \left[-2C_{ox}A + \frac{2C_{ox}(1 + e_{vx}) \left(\frac{U\sqrt{A^2 + U^2} + A_2 \ln(U + \sqrt{A^2 + U^2})}{2} \right)}{e_{vx}} \right] \quad (4.11)$$

where W denotes channel width and C_{ox} denotes oxide capacitance, and variables A , U and e_{vx} are determined by

$$A = \frac{2C_{ox}v_t^2}{Q_0} \quad (4.12)$$

$$U = 2v_t \ln(1 + e_{vx}) \quad (4.13)$$

$$e_{vx} = e^{\frac{V_{GS} - V_{TH} + \Delta V_{TH} - V}{2V_t}} \quad (4.14)$$

4.2.3 Simulation

DeckBuild was used to simulate the electrical characteristics of the 30 nm Ge Fin-FET. DeckBuild which is part of the Silvaco family, simulates and generates the device structure. It provides an interactive, graphic run-time conditions for structure developing and simulation. Drift diffusion model is used to come up with the device structure. The simulation details are mostly stated in Section 4.2, with Table 4.1 detailing the simulation pattern and material chosen for each region. I-V curves are used to study electrical characteristics, primarily on/off current ratio ($I_{ON/OFF}$) and threshold voltage (V_{TH}), which are affected by parameter variation. The effects of the following multiple design parameters are investigated in this work: fixed charge, doping concentration, and nc300 or nv300. The ranges that were used during parameter variation are stated in Table 4.2. Most of the data used for investigation is extracted from the TonyPlot outputs. TonyPlot was used to visualize both 1D and 2D structures generated by Silvaco simulators, in this case, DeckBuild. Its multiple features enabled a clear study of I-V characteristics such as cut-lines and integration of logarithmic scale. Data provided by TonyPlot was further exported to Origin for comparative analysis. Origin provides a better data analysis environment, as it allows multiple graphing, multiple colours and markers to show vector motion.

4.3 Chapter Summary

A 30 nm Ge-FinFET is designed using Silvaco software products by parameter optimization. Fixed charge, doping concentration, and nc300 or nv300 are all varied to see how each parameter affects the device's behavior. In the comparative analysis stage of the methodology, fixed charge, doping concentration, and nc300 or nv300 are all varied to see how each parameter affects the device's behavior, and

this is done through investigation of I-V curves. Table 4.2 lists all other fixed design parameters that were determined based on literature and related works. Optimal values or ranges can be determined using the On/Off current ratio and the threshold potential. Channel length and gate length are used interchangeably although mathematically the channel length is a little bit less due to side diffusion of implanted ions. The assumption is that the motion of electrons is in a single direction and Fermi potential defines the surface potential along the channel while ϕ_{ms} doesn't change but moves in the opposite direction. Movement of electrons in the narrow germanium film leads to quantum effects while surface potential promotes quantum confinement. Poisson-Schrodinger equation is used to come up with the quantum characteristics of the MOSFET with aid of the variational approach. It is also a good platform to look at the relationship of the wave function and electron density. The inversion charge carriers that are confined are not influenced by thickness [70].

Chapter 5

Results and Discussions

5.1 I-V Characteristics

5.1.1 On and Off Current Ratio

In order to successfully achieve the main aim of this work, the $I_{ON/OFF}$ and V_{TH} performances of the device have to be optimized using parameter variation. $I_{ON/OFF}$ is the figure of merit for high performance and low leakage power for the CMOS devices, which means more on-state current (I_{ON}) and less leakage power which can be achieved with low off-state current (I_{OFF}). With a higher $I_{ON/OFF}$, better gate control is guaranteed. Figure 5.1a and Figure 5.1b graphs show a well defined view of linear, pinch-off and saturation regions. The pinch-off voltage is V_{DS} , after which I_{DS} becomes almost constant; when I_{DS} becomes constant, the FET is thought to be in the saturation region, which is only defined when $V_{GS} = 0$ [12]. For this device, the gate source voltage is in the range $0.05V \leq V_{GS} \leq 1V$. Device performs well at low voltages but breaks down at higher drain voltages, when $V_{DS} \geq 4V$, at this point there is no pinch-off and over-heating occurs. This work is mainly focused on the linear region (see Figure 5.1a).

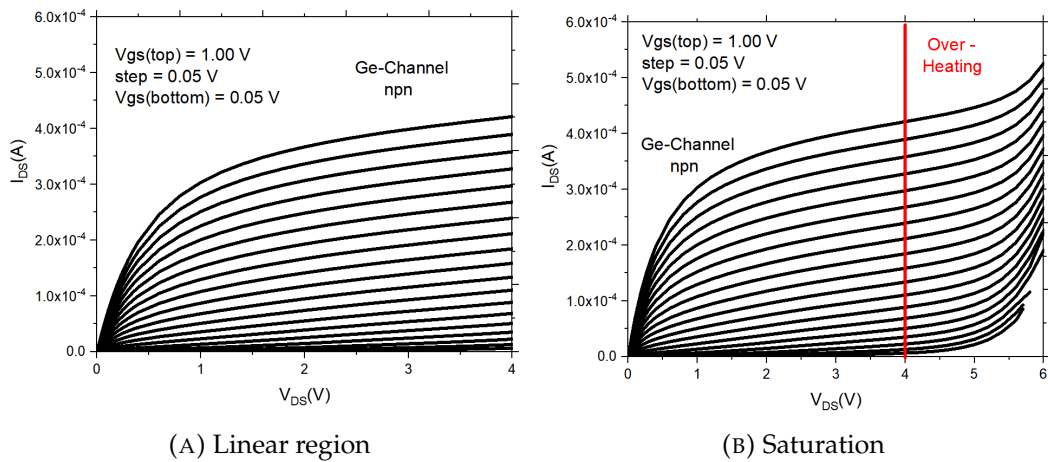


FIGURE 5.1: I-V characteristics trends - I_{DS} vs V_{DS}

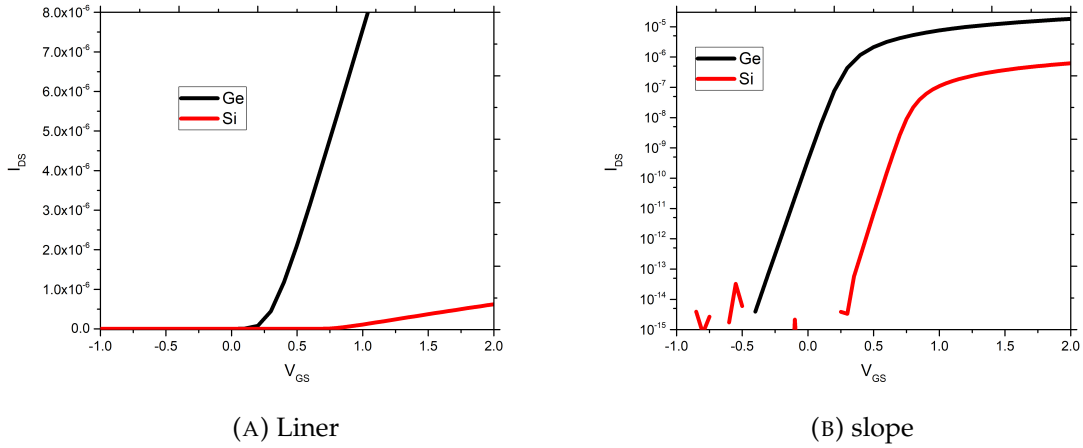


FIGURE 5.2: I-V characteristics showing differences in threshold voltages between germanium and silicon.

As stated earlier in Chapter 1, germanium has a much lower threshold potential than silicon. Figure 5.2 depicts the stark contrast between the two. The germanium device being developed in this work has higher power efficiency. This is because V_{TH} is the voltage required for the device to begin operating. This means $V_{TH} = V_{GS}$ at the beginning of the linear region, that is when the curves start to bend upwards in Figure 5.2a. This means that a germanium device will require less power to start, which appears to be a contraction of the earlier statement that stated a lower threshold as a disadvantage. To avoid scaling issues in the form of tunnelling, the threshold voltage should be lower than that of silicon but greater than the theoretical 0.3 V. Figure 5.2b shows that there is current flowing in the germanium device at $V_{GS} = 0$, but it is very small, in the order of 10^{-11} , which is approximately 0. This is the off-state current caused by tunnelling. Silicon is popular and is still widely used today, so drastically lowering the V_{TH} from 0.7 V to 0.3 V would result in significant fabrication challenges, which would still result in SCEs.

Figure 5.3 shows the I_{ON} and I_{OFF} in the linear region for the device. A device working as a switch conducts with I_{ON} when it is on and I_{OFF} when it is off. Ideally, $I_{OFF} = 0$ but for novel devices such as FinFET (solid state switches), $I_{OFF} \neq 0$ but it's considered to be very small, $I_{OFF} \ll I_{ON}$. I_{OFF} is the current passing in the device when $V_{GS} = 0$ and $V_{DS} = V_{DD}$.

The $I_{ON/OFF}$ value can be determined through calculation using Figure 5.4. Earlier research showed that $I_{ON/OFF}$ for FET, falls in the range $10^6 < I_{ON/OFF} < 10^{10}$ [12]. Recent studies [119] have found values above this range, such as $I_{ON/OFF} = 10^{12}$, which was a record at the time of publication. Technically, silicon outweighs

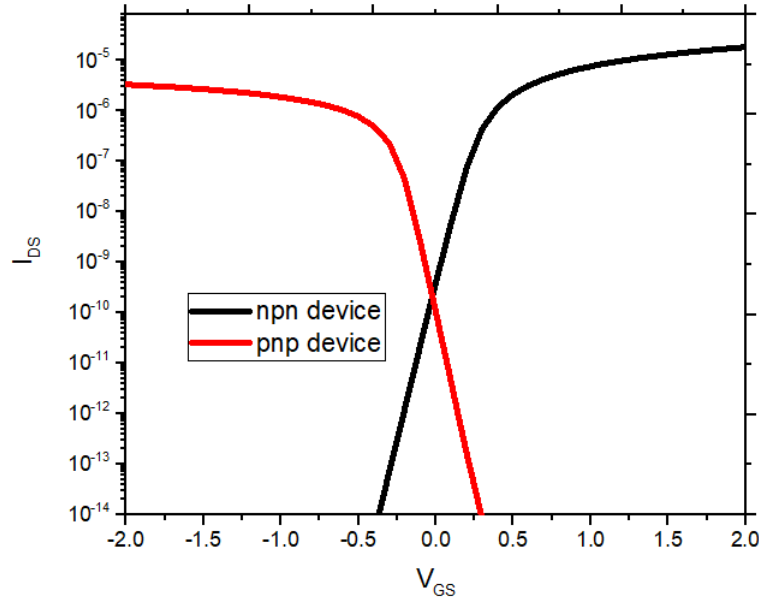


FIGURE 5.3: I-V characteristics trends showing $I_{ON/OFF}$ for both n-type and p-type in logarithmic scale

germanium 0.7V to 0.3V when it comes to threshold voltage [12]. V_{GS} required to create a conducting path between the source and drain terminals is referred to as the threshold voltage. It is the point at which the graph begins to flatten on a logarithmic scale (when $V_{TH} = V_{GS}$ and $I_{DS} \neq 0$ but $I_{DS} > 0$). It is evident from Figure 5.4b and Figure 5.4d that concentrations that can give $V_{TH} \approx 0.3V$ are $n_d = 1 \times 10^{18}$ (yellow line on Figure 5.4b) and $n_d = 1.22 \times 10^{18}$ (green line on Figure 5.4d) respectively. The yellow line of $n_d = 1 \times 10^{18}$ is not visible in Fig 5.3d because it is so close to the green line of $n_d = 1.22 \times 10^{18}$ that the green line is on top of the yellow one, as if it is overwriting it, demonstrating that they are identical. This is not surprising given the close proximity of the concentrations, a significant difference, such as $n_d = 1 \times 10^{18}$ and $n_d = 2 \times 10^{18}$, is required for a significant change to be recorded. Because other concentration values are not recorded, it can be assumed that a concentration that gives a threshold potential close to the theoretical value is in the range $1 \times 10^{18} \leq n_d \leq 1.22 \times 10^{18}$ and values closely below or above this range. A reasonable assumption would be $n_d \approx 1 \times 10^{18}$. Since $n_d = p_a$, there is no restriction on whether one uses n-type (Figure 5.4b) or p-type (Figure 5.4d). Using Figure 5.4b for calculation reference, $I_{OFF} = I_{DS}$ when $V_{GS} = 0$ and $I_{ON} = \left(\mu C_{ox} \frac{W}{2L_C} \right) (V_{GS} - V_{TH})^2 = I_{DS_{sat}}$.

$$I_{ON/OFF} = \frac{I_{ON}}{I_{OFF}} = \frac{10^{-5}}{10^{-12}} = 10^7 \quad (5.1)$$

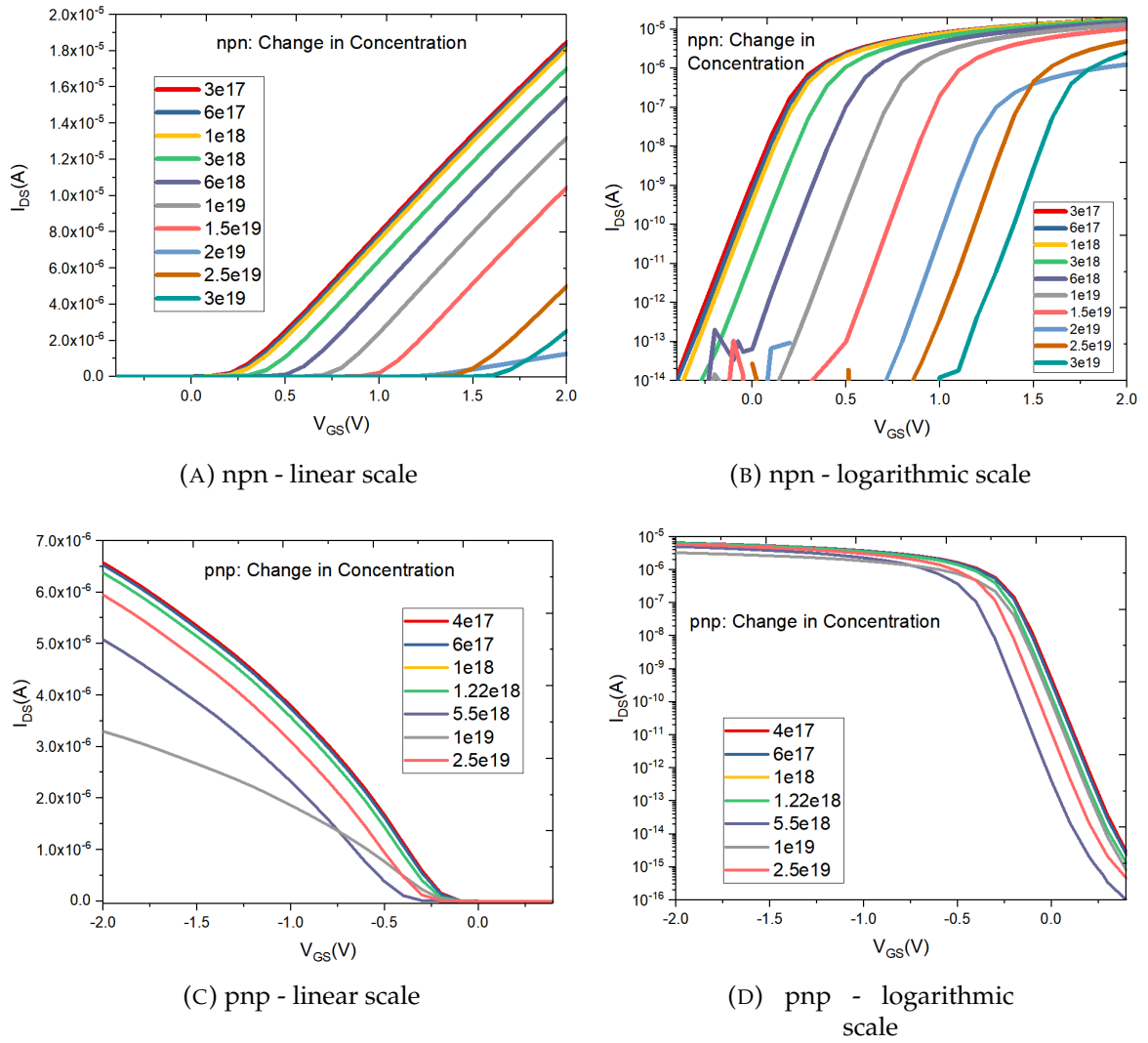


FIGURE 5.4: I-V characteristics trends - change in carrier concentration

5.1.2 Threshold Voltage

The fundamental assumption [12] of the metal-oxide semiconductor capacitor interpretation is that there is no inversion layer charge underneath the V_{TH} . This results in a zero current underneath the threshold. The exact sub-threshold current isn't really null, but rather decreases exponentially underneath the V_{TH} as follows:

$$I_D \propto e^{\frac{V_G - V_{TH}}{nV_{TH}}} \quad (5.2)$$

Equation 5.1 is the ratio of current in accumulation mode over depletion mode. $I_{ON/OFF}$ ratio must be maximized in order to suppress static transistor losses and to ensure a better gate control [119]. At $n_d = p_a > 1 \times 10^{18}$, $I_{ON/OFF}$ will improve but

high drain voltage will be required leading to SCEs in the form of velocity saturation, thus diminishing the switching speed [12]. Carrier velocity will saturate near the drain end due to the large lateral electric field provided by the high drain voltages [11]. This unwanted situation provides a case where carrier velocities adjacent to the source and drain ends behave in different ways [12]. The channel should be controlled by the gate electric field instead of being highly controlled by the drain electric field [70]. The goal is to make sure the drain electric field should have less impact on the channel.

Other than velocity saturation, I_{OFF} increases due to other SCEs as FinFETs are further scaled down, the most common being drain induced barrier lowering (DIBL). DIBL can be viewed as the reduction of V_{TH} [15] but in depth it can be viewed as the impact V_D has on the yield conductance (G_O) and the measured V_{TH} [38]. This SCE surfaces in gadgets where only L_G is scaled down without properly scaling the other transistor dimensions. Because the best possible $I_{ON/OFF}$ is found when $n_d = 1 \times 10^{18}$, a value determined based on the theoretical value of $V_{TH} = 0.3V$, at this concentration $V_{TH} = 0.37V$. As previously stated, $V_{TH} = V_{GS}$ when $I_{DS} \neq 0$, which is when the green line begins to bend upwards (see Figure 5.4a), and $V_{GS} = 0.37V$ at that point. The practical value is 0.7V higher than the theoretical value, a slight improvement that can be viewed as a positive given that the main disadvantage of germanium is its low threshold potential, as stated earlier in section 1.

It can be observed from equation 5.2 and 5.3 that the threshold variation is caused by an increase in current with increased V_D as the applied V_D controls the inversion layer charge at the drain, thereby competing with V_G . Since this impact is caused by the two-dimensional field conveyance at the drain end, it can be minimized by proper scaling of the drain and source depths subsequently increasing the SiO_2 doping density. The yield conductance of the device is in the order 10^{-4} and by looking at the size of the transistor, the density of the conductive current in response to an applied gate electric field (E_G) has been improved.

Practically for linear I-V characteristics, DIBL is found by

$$-DIBL = \frac{V_{THsat} - V_{THlow}}{V_{DD} - V_{Dlow}} \quad (5.3)$$

V_{THsat} and V_{THlow} are threshold voltages measured at supply voltage (V_{DD}), V_{THsat} at a high drain voltage while V_{THlow} is at a low drain voltage. The negative sign ensures a positive outcome since always $V_{THsat} < V_{THlow}$. $V_{DD} = 5V$ for $n_d = 1 \times 10^{18}$ and the two threshold voltages are 0.3V and 0.45V. This means $DIBL=0.031$

since $V_{D_{low}} = 0.1V$. The difference between the threshold voltages should be small in order to have low DIBL. A high DIBL leads to reduction in device operating frequency, f leading to low switching speed. DIBL value has to be kept to an absolute minimum in order to keep the switching speed at maximum.

$$-\frac{\Delta f}{f} = \frac{2DIBL}{V_{DD} - V_{TH}} \quad (5.4)$$

Δf is the frequency deviation and is directly proportional to DIBL ($\Delta f \propto DIBL$). A lower f value is desirable since it directly proportional to DIBL.

5.2 Analysis of Effects of Other Electrical and Design Parameters

V_G is related to the surface potential. The surface will have greater electric fields when the device is downscaled much further ($L_G < 30nm$). This will further force the electron wave-function into the oxide, resulting in field dependent mobility. The mobility at the surface changes in response to the electric field. When the electron wave-function extends into the oxide, carrier mobility decreases due to the oxide's lower mobility. As a result, in most cases of sub-nano CMOS VSLI, mobility throughout the inversion layer is significantly lesser than in bulk material.

Another issue with further scaling down is that the gate-oxide is also scaled down (reduction of t_{OX}), resulting in oxide breakdown and oxide reliability becomes a concern. Greater fields inside the SiO_2 layer promote carrier tunneling from the channel into this layer. These carriers gradually lead to degradation of the SiO_2 , eventually leading to its failure. Time-dependent destructive breakdown is the term for this process. High- k dielectrics such as hafnia or hafnium dioxide (HfO_2) can be considered over SiO_2 to tackle carrier tunneling but the issue is SiO_2 is compatible with germanium which makes fabrication much easier.

Figure 5.5 shows the net doping across the device. Doping concentration affects junction depth formation. V_{TH} is affected by the junction depth. Concentration is high on the sides of the device and lowers slightly at the centre because the source and drain windows are heavily doped during implantation (together with the n^+ polysilicon gate). As the net doping is increased, the carrier concentration (n_d/p_a) also increases. For a p-type Ge FinFET, this would result in an increase in concentration of holes in the acceptor energy state and this is shown in Figure 5.6.

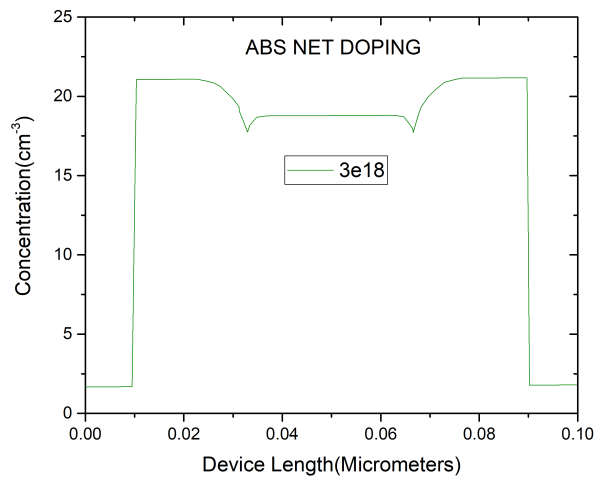


FIGURE 5.5: Net doping against concentration

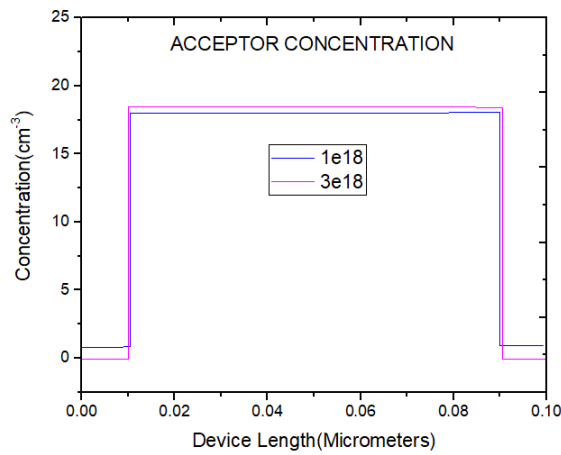


FIGURE 5.6: Acceptor Concentration

The substrate is made of germanium, and the oxide is made of silica; the difference in materials result in the formation of two distinct threshold voltages, as there is an interface between the two (the Ge-SiO₂ interface). Due to charge-sharing effects between two neighbouring gates, it has long been known that early inversion can develop at the corners of SOI frameworks [12]. The occurrence of corners can reduce a device's sub-threshold performance. The issue is avoided by placing a hard mask on top of the device [12]. To make matters more complicated, the radius of curvature of the corners has a massive effect on the device's electronic properties and can determine whether or not a distinct V_{TH} would be quantified at the device's corners and two-dimensional interfaces [12].

5.3 Chapter Summary

The new device's engineering was particularly concerned with two requirements: low power consumption and compatibility with high performance systems. This was accomplished by introducing a channel with high carrier mobility. These germanium-based carrier-transport-enhanced channel offer greater I_{ON} due to higher velocity and, on top of that, it reduces V_{DD} under a constant value of I_{ON} , which means the gate capacitance is reduced.

Chapter 6

Summary and Future Directions

A Ge channelled FinFET has been designed using Silvaco software by parameter optimization. A theoretical DG quantum analytical model was used to investigate the behaviour of a Ge based channel as three device design parameters (fixed charge, doping concentration and nc300 or nv300) are varied in order to optimize $I_{ON/OFF}$ and V_{TH} . The model is based on the quantum mechanical variational approach and accounts for the Ge channel thickness (t_{fin}) which depends on electric potential found using Poisson and Schrodinger equation. The linear region of this developed device falls in the range $0V < V_{DS} < 4V$ and at drain voltages above this range over-heating occurs.

FinFET falls under solid state switches hence $I_{OFF} \neq 0$ but is considered to be very small and passes through the device when $V_{GS} = 0$ and $V_{DS} = V_{DD}$, $I_{OFF} \ll I_{ON}$. $I_{ON/OFF} \approx 10^7$ when the device operating in the range $0.05V \leq V_{GS} \leq 1V$ and this value is reasonable because most of the FET devices operate in the range $10^6 < I_{ON/OFF} < 10^{10}$. This optimal $I_{ON/OFF}$ can only be achieved at $n_d = p_a \approx 1 \times 10^{18}$ since $n_d = p_a$. Above this value, that is $n_d = p_a > 1 \times 10^{18}$, $I_{ON/OFF}$ will increase requiring high V_D . This will lead to SCEs in the form of velocity saturation, thus diminishing the switching speed. I_{OFF} can be a result of other SCEs other than velocity saturation, the noticeable one being DIBL which is the reduction of V_{TH} but in design aspect, it is the impact of V_D on G_O . Scaling L_G without properly scaling t_{fin} and H_{fin} leads to DIBL. At optimal $I_{ON/OFF}$, practically $V_{TH} = 0.37V$, a much needed value greater than the theoretical $0.3V$, because this low threshold potential in germanium-based devices always leads to SCE, reducing switching speed. Threshold variation is caused by increase in I_D and V_D since applied V_D competes with V_G resulting in a two dimensional field conveyance at the drain end. This means that properly scaling the drain and source depths and increasing the doping density for the oxide is mandatory. At optimal environment, DIBL=0.031 (lowest value possible since $\Delta f \propto \text{DIBL}$ and inversely proportional to the switching speed), and G_O is in the order 10^{-4} . The net doping increases with

n_d/p_a .

Based on Section 5.2 we can conclude by recommending other oxides as alternatives to SiO_2 provided the compatibility issue will be addressed. These oxides are commonly referred to as high- k dielectrics. Because they have a higher dielectric constant, they can achieve the very same gate capacitance with a thicker oxide. The goal is to achieve the same level of stability, dependability, and breakdown voltage as SiO_2 . Al_2O_3 , ZrO , and TiO are among the oxides of interest.

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