RESEARCH & INNOVATION SYMPOSIUM 2019

ISSN: 2521-2292

# IGZO TFT versus the MOSFET

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**Abstract: Indium gallium zinc oxide thin film transistor (IGZO TFT) characteristics are investigated, improved and then compared with the standard metal-oxide semiconductor field-effect transistor (MOSFET). The device tends to operate with a negative threshold voltage which is undesirable as it means the device is 'ON' at 0.0 V. For the device to be an effective CPU switch, it needs to operate with voltage values between 0.0 V and 5.0 V where the lower value means it is completely 'OFF' with no leakage currents. Negative fixed charge was introduced to help turn the device 'OFF' whereas the MOSFET had negligible values. The TFT was driven at a drain voltage of 1.0 V whereas the MOSFET was at 0.1 V. This made the two devices comparable with similar threshold voltage of 0.6 V and an ideal subthreshold swing of 60 mV/decade. The experiment shows that the subthreshold voltage for the IGZO TFT is excellent at lower drain currents but degrades at higher currents. The quick degradation observed on the subthreshold region can also be attributed to short channel effects (SCEs).**

**Keywords: Indium gallium zinc oxide thin film transistor (IGZO TFT), metal oxide semiconductor field effect transistor (MOSFET), scaling, short channel effects (SCE)**

## I. INTRODUCTION

The metal-oxide semiconductor field-effect transistor (MOSFET) has been around for over six decades [1]. Of late the device has failed to meet the technological demands due to poor scaling properties. Ideally all dimensions are normally reduced by a factor 'k', whereas the doping is the opposite and increases by the same factor. But that has not been the case for the MOSFET, the device width and wiring dimensions have not been scaled as fast as the channel lengths. In addition, the device does not allow for voltage scaling due to subthreshold slopes, off currents, and built-in potentials that need to be maintained to avoid device degradation [1—2].

Several techniques have been developed to reduce short channel effects (SCE) which are as follows:

a) Gate (dual work function, low resistance, and tight dimensional control),
b) Insulator (very thin dimensions, reducing defect density, reducing tunnelling current, using substitute material),
c) Channel (making them shallow, strained layer to enhance mobility) [1—7].

High-K dielectrics have been introduced to replace the conventional $SiO_2$ which should help maintain acceptable-scalable dielectric thickness while keeping gate leakage currents low [1—2]. Even with so many improvements being made on the device, the limits of MOSFET scaling keep approaching. The thickness of the oxide ($t_{ox}$) cannot be less than 1nm due to higher tunnelling current and significant operational variation. The substrate doping is also very high which creates leakage and tunnelling currents that are unacceptable to device operation. The greatest physical limit in further scaling the MOSFET is the inner distance of atoms in silicon crystals which is around 0.3nm. Thus, up to a certain point, further scaling will not be realised [1—7].

Due to this scaling limit, there has been an introduction of new material and heterojunction structures as alternative to MOSFET device [2]. This paper presents indium gallium zinc oxide (IGZO) planar bulk thin film transistor (TFT) as an alternative to the MOSFET. The device has been around for over two decades [2]. The success of the device in meeting the technological demands has largely been dominated by the shrinking size of its physiognomies and junctionless (no p-n junctions) properties [1]. The junctionless property gives it an advantage over the MOSFET device especially concerning to scaling.

IGZO has practical advantages that make it an attractive semiconductor from an industrial point of view. It has low costs, abundant, non-toxic, transparent, large excitonic binding energy of 60 meV, soluble, compatible with intercellular material, and wide and direct band gap of 3.2 eV making it highly sensitive. The larger the band gap, the better is the semiconductor able to switch states and to insulate leakage currents. IGZO permittivity is 11.9 whereas ZnO permittivity is 8.12 which makes it even more preferred form of material. The higher the permittivity, the higher the output currents. The material allows for low-temperature processing of around 180°C − 210°C compared to 850°C − 1100°C for silicon. With low-temperature fabrication processes, high-quality devices can be fabricated using conventional processing technology, thereby making it suitable for low-cost mass-production [2—14].

Currently, the main commercial application for IGZO (and/or ZnO) material is in displays, with companies like Sharp and Samsung putting IGZO into mobile phone displays [9—11].

RESEARCH & INNOVATION SYMPOSIUM 2019
ISSN: 2521-2292

IGZO displays out-perform other semiconductor displays such as amorphous silicon and organic semiconductors by providing improved resolution and reduced power consumption. This is possible because IGZO has x20 to x50 times higher mobility than amorphous silicon and polymers, which allows for device scaling without affecting performance [9—11]. Higher mobility values can also be achieved with amorphous silicon technology, but it needs to be laser annealed which incur more cost in the fabrication process [9—11].

## II. SIMULATION PROCEDURE

Three Silvaco products were used: Athena, DevEdit [15] and Atlas [16]. Figure 1 shows the two (2) device structures that were developed using Athena and DevEdit, whereas electrical characteristics and bias conditions were simulated through Atlas. Athena is used mainly to develop and show the fabrication steps in virtual environment of a device whereas DevEdit is more of an integrated circuit (IC) layout editor. DevEdit is excellent at mesh specification, refinement and mask viewing. Both tools produce same results in terms of structures. The TFT structure is assumed to have a single crystal IGZO channel with parameters as stated in Table 1 and compared to the MOSFET.

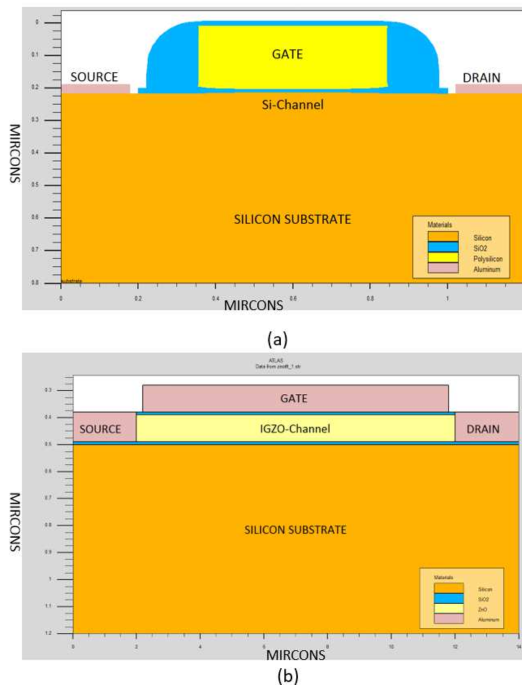


Fig. 1: Structures simulated (a) MOSFET (b) IGZO TFT

Under ATLAS, the physical model used is the Boltzmann model which is sufficient in this case because the other models are for specific situations such as heavily doped regions, low temperatures that tend to freeze the carriers, and for bipolar transistors. For mobility models, Atlas used the default values which are entirely isotropic in nature and there is no directional component. IGZO is a new material and ATLAS software does not provide for IGZO mobility models. For recombination models, the Shockley-Read-hall (SRH) model was utilized as it is the most general model for simulating new materials [10, 16—18].

Table 1: Parameters used for IGZO TFT Simulation; All simulation parameters were defined to be the same as the experimental device.

| No. | Physical Parameter | MOSFET | IGZO TFT | Units |
|---|---|---|---|---|
| 1 | Si Substrate Doping | $1.32 \times 10^{15}$ | $1.32 \times 10^{15}$ | $cm^{-3}$ |
| 2 | L = Length of channel | $0.5 \times 10^{-6}$ | $10.0 \times 10^{-6}$ | m |
| 3 | $T_{ZnO}$ = Thickness of channel | $0.3 \times 10^{-6}$ | $0.1 \times 10^{-6}$ | m |
| 4 | W = Z = Width of channel | $1.0 \times 10^{-6}$ | $1.0 \times 10^{-6}$ | m |
| 5 | $SiO_2$ Insulator thickness (d) | $0.05 \times 10^{-6}$ | $10.0 \times 10^{-9}$ | m |
| 6 | Si Substrate thickness | $0.6 \times 10^{-6}$ | $0.7 \times 10^{-6}$ | m |

## III. RESULTS AND DISCUSSION

Figure 2 shows the $I_{DS} – V_{GS}$ plot of the TFT structure. It was observed that the IGZO TFT tends to operate with negative voltage based on its subthreshold region. This is undesirable as it means the device is 'ON' at 0.0 V. For the device to be an effective CPU switch, it needs to operate with voltage values between 0.0 V and 5.0 V where the lower value means it is completely 'OFF' with no leakage currents. Negative fixed charge was introduced to help turn the device 'OFF'. Figure 2 shows that increasing negative fixed charge from -3.0 x $10^{10}$ $cm^{-2}$ to -1.0 x $10^{12}$ $cm^{-2}$ slowly minimizes the leakage currents and brought the device into desired operational voltage. This change comes with unintended consequences of decreasing the maximum currents as shown in Figure 2(a) and degrading the subthreshold slope (shown in Figure 2b). The quick degradation observed on the subthreshold region can also be attributed to short channel effects (SCEs). This is because SCEs tend to negatively impact the current and also weaken the subthreshold slope [7].

Change in drain voltage was then used to mitigate the unintended consequences of introducing negative fixed charge. Figure 3 shows that the values were changed from 0.1 V to 1.5 V in steps of 0.2 V. The effects are highly desired as drain current was increased without adverse consequences (all other traits remain constant). An increase in drain voltage is desired and must be done with caution to minimize overheating of the device. Overheating degrades the maximum current of the device and damages it over time.

ISSN: 2521-2292

Figure 4 shows the comparison of drain current against gate voltage between IGZO TFT with the standard MOSFET. The graphs depict linear and subthreshold regions. As noted, the MOSFET is simulated under ideal conditions, therefore it has ideal characteristics. To achieve results similar to the ideal MOSFET, the TFT is driven at 1.0 V whereas it is at 0.1 V. This is a disadvantage for the TFT as it is desirable to drive devices with low voltage which can produce high currents. The IGZO TFT also has high fixed charge of -2.0 x $10^{11}$ $cm^{-2}$ whereas the MOSFET has an ideal value of -3.0 x $10^{10}$ $cm^{-2}$. The two devices have a similar threshold voltage of roughly 0.6 V and an ideal subthreshold voltage 60 mV/decade. Figure 4(a) shows that the MOSFET linear region is bending and is starting to saturate whereas the IGZO TFT shows strength in continuing the linear region further. Figure 4(b) shows that the subthreshold voltage for the IGZO TFT is excellent at lower drain currents but degrades at higher currents.

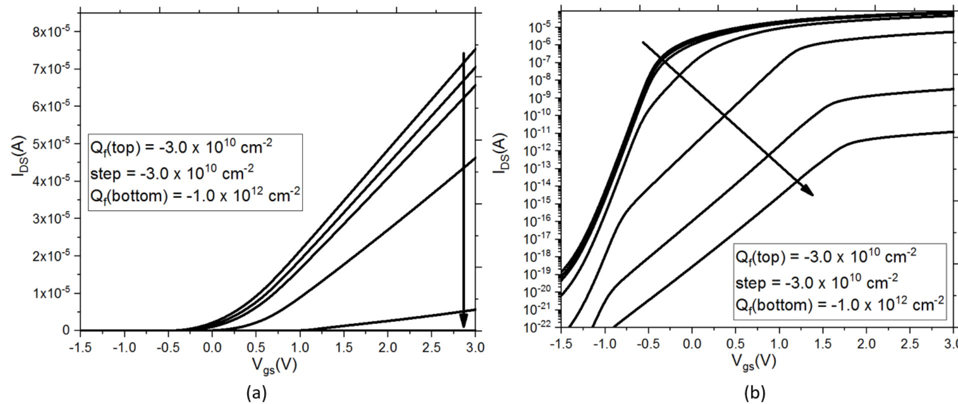


Fig. 2: A plot of drain current versus gate voltage showing the effect of the IGZO TFT fixed charge as it is varied from 3.0 x $10^{10}$ $cm^{-2}$ to 1.0 x $10^{12}$ $cm^{-2}$ in steps of 3.0 x $10^{10}$ $cm^{-2}$: (a) in the linear region (b) in the subthreshold region.

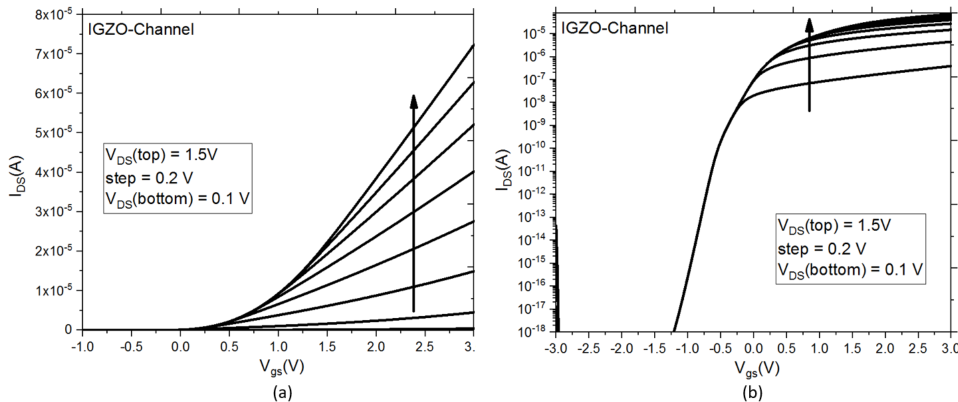


Fig. 3: A plot of drain current versus gate voltage showing the effect of the IGZO TFT drain voltage as it is varied from 0.1 V to 1.5 V in steps of 0.2 V: (a) in the linear region (b) in the subthreshold region. The fixed charge is at -1.0 x$10^{12}$ $cm^{-2}$.

ISSN: 2521-2292

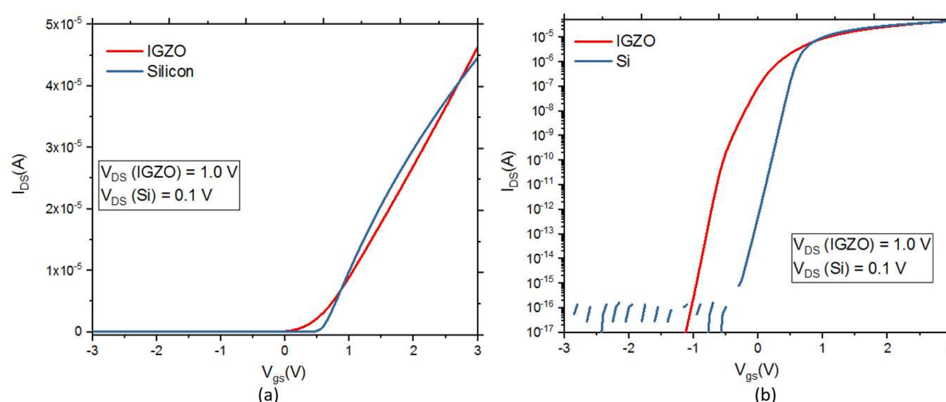


Fig. 4: A plot of drain current versus gate voltage comparing IGZO TFT with the standard MOSFET. The MOSFET is driven at a lower voltage of $V_{DS}$ =0.1 V whereas the TFT is being driven at a higher voltage of $V_{DS}$ = 1.0 V. The graphs depict (a) in the linear region (b) in the subthreshold region

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## IV. CONCLUSION

In summary, IGZO TFT performance has been investigated, improved and then compared with the standard MOSFET. The subthreshold swing of IGZO TFT degraded quickly when negative fixed charge increased from -3.0 x $10^{10}$ $cm^{-2}$ to -1.0 x$10^{12}$ $cm^{-2}$ due to short channel effects. At an oxide fixed charge of 2.0 x $10^{11}$ $cm^{-2}$ and at $V_{DS}$ = 1 V, the IGZO TFT exhibits similar threshold voltage of ~0.6V and subthreshold swing of ~60 mV/decade with standard MOSFE at $V_{DS}$ =0.1V. With further scaling, the device can compete with the FinFET and nanowire-FET silicon devices.

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